CA-IF1145 High-speed CAN Transceiver with Partial Networking

1. Features

- Meets the requirements of ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 physical layer standards
- Optimized for high-speed CAN communication and CAN FD tolerance enables CAN FD data transmission up to 5 Mbit/s
- Supports selective wake to wake-up partial networking nodes
- CAN bus pins short-circuit protection to ±42 V, ideal for 12V battery systems
- 2.85V to 5.5V logic-supply (V_{IO}) range easy to interface with 3.3V and 5.0V logic
- Autonomous bus biasing
- Advanced ECU power management
  - INH output can be used to turn-off entire node to reduce power consumption
  - Low-power standby and sleep modes support both remote wake-up and local wake-up
  - Remote wake-up via standard CAN wake-up pattern(WUP) or selective wake-up frame (WUF) according to ISO 11898-2:2016
  - Selective wake supports 50 kbit/s, 100 kbit/s, 125 kbit/s, 250 kbit/s, 500 kbit/s and 1 Mbit/s CAN bit-rate
  - Local wake-up via WAKE terminal, also local wake-up can be disabled to reduce power consumption
  - Wake-up sources identification
- Integrated protection and diagnosis increase system robustness
  - Battery and CAN bus pins protected against transients according to ISO 7637-3, test pulses 1, 2a, 3a and 3b
  - Ideal passive behavior when unpowered: bus terminals are high impedance
  - Overtemperature shutdown and alarm
  - Undervoltage protection on VCC, BAT and VIO supply terminals
  - Cold start-up detection (PO and NMS bits)
  - Transmitter dominant timeout prevents lockup
  - Advanced interrupt sources diagnosis
  - 16/24/32 bit SPI-compatible interface for device configuration, control and events diagnosis
- –55°C to 150°C junction temperature range
- Available in SOIC14 and DFN14 packages

2. Applications

- Body electronics
- In-car entertainment systems
- Hybrid, electric and power train system
- Smart ADAS
- Chassis systems

3. General Description

The CA-IF1145 devices are robust high-speed, low-power control area network (CAN) transceivers with integrated protection for automotive applications. These devices meet the requirements ISO1189-2:2016 and SAE J2284-1 to SAE J2284-5 physical layer standards. All devices feature up to ±42V extended fault protection on the data transmission lines in all operation modes.

The CA-IF1145 devices can operate in different modes: normal operation, overtemperature protection mode, and standby, sleep, off modes for low current consumption, as well as wake-up capability over CAN bus or via the local WAKE pin. A selective wake-up (FD-passive) is able to ignore CAN FD(flexible data rate) frames while waiting for a valid wake-up frame in sleep or standby modes to support ISO 11898-2:2016 compliant CAN partial networking and enables reliable communication in the CAN FD networks up to 5 Mbit/s data rates. Inhibit output (INH) can be used to control one or more external voltage regulators presented on a node to reduce the battery power consumption at system level. The CA-IF1145 features ideal passive behavior when unpowered, all bus terminals are high impedance during power-off. These make the CA-IF1145 ideal in the applications that all nodes are always connected to the power supply line, because the transceivers can be active only as required to minimize system current consumption.

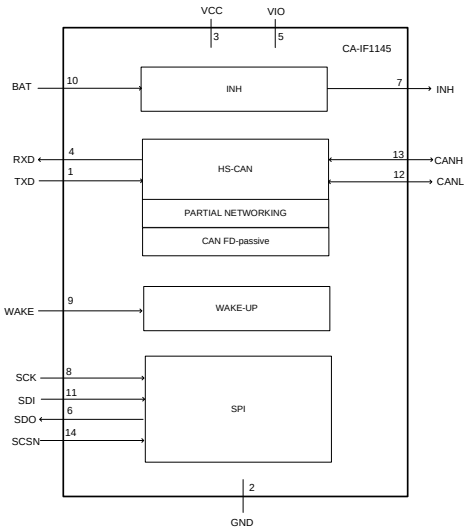
The CA-IF1145 series devices include a dominant timeout detection to prevent bus lockup caused by controller error or by a fault on the TXD input. Also, the CA-IF1145 devices feature individual logic supply input (VIO) and provide low level translation to simplify the interface with low voltage CAN controllers. SPI-compatible interface is available for transceiver operation control and status information reading.

The CA-IF1145 family of devices is available in a standard 14-pin narrow-body SOIC package and 14-pin DFN package, operates over the -55°C to +150°C junction temperature range.

Device Information

Part number	Package	Package size(NOM)
CA-IF1145FNF-Q1	SOIC14(NF)	3.9mm x 8.65mm
CA-IF1145FDF-Q1	DFN14(DF)	3.0mm x 4.5mm

Simplified Block Diagram



4. Ordering Information

Table 4-1. Ordering Information

Part Number	Features	Package	Package size
CA-IF1145FNF-Q1	Ignore CAN FD frames in sleep mode	SOIC14	3.9mm x 8.65mm
CA-IF1145FDF-Q1	Ignore CAN FD frames in sleep mode	DFN14	3.0mm x 4.5mm

Contents

5. Revision History

Revision Number	Description	Page Changed
Ver.1.0	NA	

6. Pin Configuration and Functions

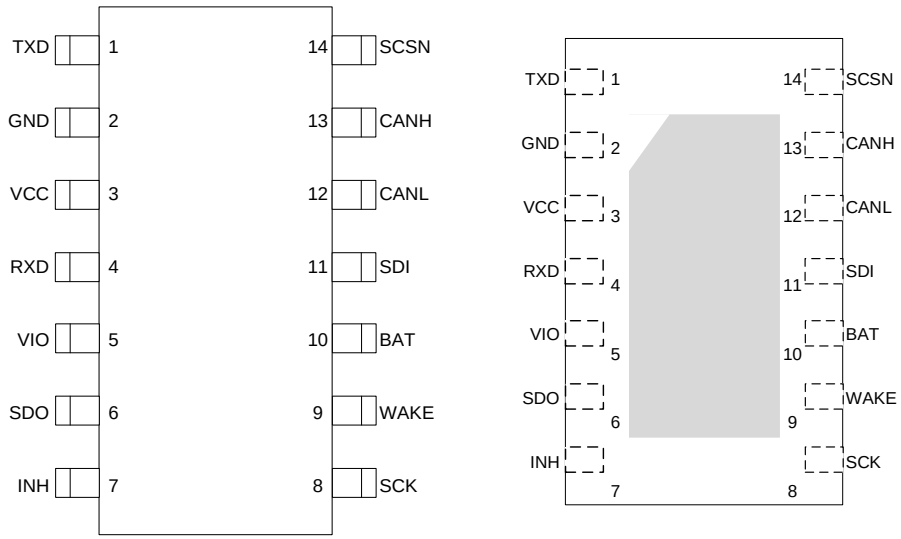


Figure 6-1. CA-IF1145 pin configuration

Table 6-1. CA-IF1145 pin configuration and description

Pin Name	Pin#	Type	Description
TXD	1	Digital input	Transmit Data Input. In normal operation, drive TXD high to set the driver in the recessive state; drive TXD low to set the driver in the dominant state. TXD is a CMOS/TTL compatible input from a CAN controller with an internal pull-up to VIO.
GND	2	GND	Ground.
VCC	3	Power	+5V Supply Voltage. Bypass VCC to GND with an at least 0.1µF capacitor.
RXD	4	Digital output	Receive Data Output. In normal operation, RXD is low for dominant bus state and high for recessive bus state. RXD is a CMOS/TTL compatible output from the bus lines CANH and CANL.
VIO	5	Power	I/O Logic Supply Input. VIO input is the logic supply voltage for the logic input/output between the CAN transceiver and controller. VIO allows full compatibility from +2.85V to +5.5V logic on all digital lines. Bypass VIO to GND with a 0.1µF capacitor. Connect VIO to VCC for +5V logic compatibility.
SDO	6	Digital output	SPI Serial Data Output. Data is updated on the falling edge of SCK. When SCSN is high, SDO is high-impedance.
INH	7	High-voltage output	Inhibit Output. INH can be used to control external voltage regulators or/and microcontroller to reduce system power consumption.
SCK	8	Digital input	SPI Serial Clock Input. SCK has internal pull-down.
WAKE	9	High-voltage input	Local Wake-up Input. If enabled, either a low-to-high(rising edge) or a high-to-low(falling edge) transition will generate a local wake-up event. Pull WAKE to ground to avoid unwanted wake-up events if not used.
BAT	10	Power	Battery Supply Input.
SDI	11	Digital input	SPI Serial Data Input. Data is clocked into SDI on the rising edge of SCK.
CANL	12	Bus I/O	CAN bus line low.
CANH	13	Bus I/O	CAN bus line high.
SCSN	14	Digital input	SPI Chip-Select Input. Assert low to latch input states and enable the SPI interface.

7. Specifications

7.1. Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
V_{BAT}	Battery supply voltage range	-0.3	42	V
V_{CC}	5V bus supply voltage range	-0.3	6	V
V_{IO}	I/O logic supply voltage range	-0.3	6	V
V_{BUS}	CAN bus I/O voltage range (CANH,CANL)	-42	42	V
$V_{(DIFF)}$	Max differential voltage between CANH and CANL	-42	42	V
$V_{(Logic\_Input)}$	Logic input terminal voltage range (TXD, SDI, SCK, SCSN)	-0.3	V_{IO}+0.3	V
$V_{(Logic\_Output)}$	Logic output terminal voltage range (RXD)	-0.3	V_{IO}+0.3	V
V_{INH}	INH Output voltage range	-42	42	V
$V_{(wake)}$	WAKE input voltage range	-42	42	V
$I_{O(LOGIC)}$	Logic output current (RXD)		5	mA
$I_{O(INH)}$	INH output current		6	mA
$I_{O(WAKE)}$	WAKE input current		1	mA
T_J	Virtual junction temperature range	-55	150	℃

Note:
The stresses listed under “Absolute Maximum Ratings” are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.

7.2. ESD Ratings

Parameters	TEST CONDITIONS		VALUE	UNIT
CA-IF1145NF-Q1, CA-IF1145DF-Q1				
HBM ESD	CAN bus terminals (CANH, CANL) to GND		±8000	V
	Other pins		±2000	
CDM ESD	All pins		±1500	V
System Level ESD	CAN bus terminals (CANH, CANL) to GND VBAT, WAKE terminals to GND	IEC 61000-4-2: unpowered contact discharge.	±6000	V
ISO7637 transient according to GIFT-ICT CAN EMC test	CAN bus terminals (CANH, CANL) to GND VBAT, WAKE terminals to GND	Pulse 1	-100	V
		Pulse 2	+75	V
		Pulse 3a	-150	V
		Pulse 3b	+100	V
ISO7637-3 transient	CAN bus terminals (CANH, CANL) to GND VBAT, WAKE terminals to GND	Direct coupling 100nF capacitor "slow transient pulse" – powered.	±85	V

Note:
Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.

7.3. Recommended Operating Conditions

PARAMETER		MIN	MAX	UNIT
V_{bat}	Battery supply voltage range	4.5	28	V
V_{CC}	5-V bus supply voltage	4.5	5.5	V
V_{IO}	I/O logic supply voltage range	2.85	5.5	V
I_{OH}(RXD)	RXD terminal high level output current	-2		mA
I_{OL}(RXD)	RXD terminal low level output current		2	mA
I_O(INH)	INH output current		2	mA
T_A	Ambient temperature	-40	125	℃

7.4. Thermal Information

Thermal Metric		CA-IF1145		UNIT
		SOIC14	DFN14	
$R_{\theta JA}$	IC junction to ambient	76.6	35.1	°C/W

7.5. Electrical Characteristics

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
I_{BAT}	Battery Supply Current	Normal operation, MC=111		0.35	1	mA
		Sleep mode, MC=001； CWE=1； CAN bus offline mode; VBAT=7V to 18V		60		μA
		Standby mode, MC=100； CWE=1； CAN bus offline mode; VBAT=7V to 18V		85	117	μA
		CAN bus offline bias mode.		500	590	μA
		CAN offline bias mode with active partial networking decoder		1	1.2	mA
I_{cc}	VCC Supply Current	TXD=VIO, RL=60 Ohm(recessive)		3.3	4.5	mA
		TXD=0V, RL=60 Ohm (dominant)		54	65	mA
		Normal mode, dominant, TXD=0V, -3V<CANH=CANL<18V, R_L open		78	95	mA
		Standby mode, disable selective wake-up		2.4	4	μA
		Sleep mode		2.4	4.2	μA
I_{IO}	I/O Supply Current	Standby mode, TXD=V_{IO}		6.1	10	μA
		Sleep mode, TXD=V_{IO}		6.1	14	μA
$V_{th(det)pon}$	BAT power-on detection	Rising	3.4		4.4	V
$V_{th(det)poff}$	BAT power-off detection	Falling	2.3		3	V
$V_{UVR(CAN)}$	CAN UVLO recovery voltage	Rising	3.2		4.35	V
$V_{UVD(CAN)}$	CAN UVLO threshold	Falling	3.1		3.9	V
$V_{UVR(VCC)}$	VCC UVLO threshold	Rising	3.3		4.6	V
$V_{UVD(VCC)}$	VCC UVLO threshold	Falling	3		4.3	V
$V_{UVR(VIO)}$	VIO UVLO threshold	Rising	2.2		2.85	V
$V_{UVD(VIO)}$	VIO UVLO threshold	Falling	2.1		2.75	V
LOGIC INTERFACE (SDI, SCK, SCSN input)						
V_{IH}	High-level input voltage		0.7Xv_{Io}			V
V_{IL}	Low-level input voltage				0.3Xv_{Io}	V
$R_{pd(SCK)}$	SCK pull-down resistance		40	60	80	kΩ
$R_{pu(SCSN)}$	SCSN pull-up resistance		40	60	80	kΩ
$R_{pd(SDI)}$	SDI pull-down resistance	V_{SDI}<$V_{th(sw)}$	40	60	80	kΩ
$R_{pu(SDI)}$	SDI pull-up resistance	V_{SDI}>$V_{th(sw)}$	40	60	80	kΩ
LOGIC INTERFACE (SDO output)						
V_{OH}	High-level output voltage	Io=-4mA,	V_{IO}-0.4			V
V_{OL}	Low-level output voltage	Io=+4mA,			0.4	V
$I_{LO(off)}$	Leakage current at off mode	V_{SCSN}=V_{IO}, Vo=0V to V_{IO}	-5		5	μA
LOGIC INTERFACE (TXD input)						
V_{IH}	High-level input voltage		0.7Xv_{Io}			V
V_{IL}	Low-level input voltage				0.3xV_{io}	V
$R_{pu(TXD)}$	TXD pull-up resistance		40	60	80	kΩ

Electrical Characteristics (continued)

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INTERFACE (RXD output)						
V_{OH}	High-level output voltage	Io=-4mA,	V_{IO}-0.4			V
V_{OL}	Low-level output voltage	Io=+4mA,			0.4	V
$R_{pu(RXD)}$	RXD pull-up resistance	Vsup UVLO or sleep mode	40	60	80	kΩ
INH INTERFACE (INH output)						
ΔV_H	High level voltage drop, INH to V_{BAT}	I_{INH}=-180μA,	0		0.8	V
$R_{pd(INH)}$	Pull-down resistance	Sleep mode		3		MΩ
Io(sc)	Short-circuit current	V_{INH}=0V	-15	-4		mA
WAKE INTERFACE (WAKE input)						
V_{IH}	High-level input voltage	Standby mode/Sleep mode	2.8		4.1	V
V_{IL}	Low-level input voltage	Standby mode/sleep mode	2.4		3.75	V
V_{hys}	Input threshold hysteresis		150		800	mV
I_{IL}	Low-level input leakage current	WAKE=5V			1.5	μA
CAN BUS DRIVER						
$V_{O(DOM)}$	Bus output voltage (dominant)	TXD=Low, RL=50 -65Ohm, CANH, see Figure 8-1	2.75	3.5	4.5	V
		TXD=Low, RL=50 -65Ohm, CANL, see Figure 8-1	0.5	1.5	2.25	V
$V_{O(DOM)}$	Bus output differential voltage (dominant)	TXD=Low, RL=45-70 Ohm, RCM open, see Figure 8-1	1.5		3	V
		TXD=Low, RL=2240 Ohm, RCM open, see Figure 8-1	1.5		5	V
$V_{O(REC)}$	Bus output voltage (recessive)	CAN active, TXD=High, no load, CANH/CANL, see Figure 8-1	2	0.5xV_{CC}	3	V
		CAN offline bias/listen-only mode, TXD=High, no load, CANH/CANL, see Figure 8-1	2	2.5	3	V
		CAN offline mode, TXD=High, no load, CANH/CANL, see Figure 8-1	-0.1		0.1	V
$V_{OD(REC)}$	Bus output differential voltage (recessive)	CAN active/offline bias/listen-only mode, TXD=High, no load, CANH/CANL, see Figure 8-1	-50		50	mV
		CAN offline mode, TXD=High, no load, CANH/CANL, see Figure 8-1	-200		200	mV
$I_{OS(SS\_DOM)}$	Short-circuit current (dominant)	TXD=Low, CANL open, CANH from -15V to 27V, see Figure 8-7	-95		6	mA
		TXD=Low, C ANH open, CANL from -15V to 27V, see Figure 8-7	-6		95	
$I_{OS(SS\_REC)}$	Short-circuit current (recessive)	TXD=High, VBUS from -27V to 32V, see Figure 8-7	-3.5		3.5	mA
V_{sym}	Transient symmetry (dominant or recessive)	RL=60 Ohm, C_{split}=4.7nF, RCM open, TXD=250kHz, 1MHz, 2.5MHz, V_{sym}=V_{CANH}+V_{CANL}	0.9xV_{CC}		1.1xV_{CC}	V
V_{sym_dc}	DC Output symmetry (dominant or recessive)	RL=60 Ohm, R_{CM} open, V_{sym_dc}=V_{CC}-V_{CANH}-V_{CANL}	-0.4		0.4	V

Electrical Characteristics (continued)

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN RECEIVER (TXD=High, CANH/CANL drive externally)						
V_{CM}	Common-mode input range	Normal mode/standby mode, RXD output valid, see Figure 8-2	-12		+12	V
V_{IT}	Input threshold voltage at active/listen-only modes	Vcm from -12V to 12V, see Figure 8-2	500		900	mV
$V_{IT(STB)}$	Input threshold voltage at offline mode	Vcm from -12V to 12V, see Figure 8-2	400		1150	mV
V_{DIFF_D}	Input differential threshold voltage at normal/listen-only modes (dominant)	Vcm from -12V to 12V, see Figure 8-2	0.9		9	V
V_{DIFF_R}	Input differential threshold voltage at normal/listen-only modes (recessive)	Vcm from -12V to 12V, see Figure 8-2	-4		0.5	V
$V_{DIFF\_D(STB)}$	Input differential threshold voltage at offline mode (dominant)	Vcm from -12V to 12V, see Figure 8-2	1.15		9	V
$V_{DIFF\_R(STB)}$	Input differential threshold voltage at offline mode (recessive)	Vcm from -12V to 12V, see Figure 8-2	-4		0.4	V
$V_{DIFF\_(HYST)}$	Differential input threshold hysteresis	Normal mode		100		mV
R_{IN}	CANH/CANL input resistance	TXD=High, STB=0V, Vcm from -30V to 30V	10	15	26	kΩ
R_{DIFF}	Differential input resistance	TXD=High, STB=0V, Vcm from -30V to 30V	20	30	52	kΩ
$R_{DIFF\ (M)}$	Input resistance matching	CANH=CANL=5V	-1.5		1.5	%
I_{LKG}	Input Leakage Current	VCC = 0V, VCAN=5V	-5		5	μA
C_{IN}	Input capacitance	CANH or CANL to GND, TXD=High		30		pF
C_{IN_DIFF}	Differential input capacitance	CANH to CANL, TXD=High		18		pF
Devices						
$T_{th(act)otp}$	Thermal shutdown temperature			175		°C
$T_{th(rel)otp}$	Thermal shutdown release threshold temperature			140		°C
$T_{th(warn)otp}$	Overtemperature alarm threshold			140		°C

7.6. Dynamic Characteristics

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
t_{ONTXD}	TXD propagation delay (recessive to dominant)	STB=0V, RL=60 Ohm, CL=100pF, see Figure 8-1		70		ns
t_{OFFTXD}	TXD propagation delay (dominant to recessive)	STB=0V, RL=60 Ohm, CL=100pF, see Figure 8-1		50		ns
RECEIVER						
t_{ONRXD}	RXD propagation delay (recessive to dominant)	STB=0V, CL=15pF, see Figure 8-2		65		ns
t_{OFFRXD}	RXD propagation delay (dominant to recessive)	STB=0V, CL=15pF, see Figure 8-2		70		ns

Dynamic Characteristics (continued)

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE						
t_{loop1}	Total loop delay, driver input (TXD) to receiver output (RXD)	recessive to dominant, RL=60 Ohm, CL=100pF, see Figure 8-3		135	210	ns
t_{loop2}	Total loop delay, driver input (TXD) to receiver output (RXD)	dominant to recessive, RL=60 Ohm, CL=100pF, see Figure 8-3		130	210	ns
$t_{wake(busdom)}$	Bus dominant wake-up time		0.5		1.8	us
$t_{wake(busrec)}$	Bus recessive wake-up time		0.5		1.8	µs
$t_{o(wake)bus}$	Bus wake-up timeout		0.8		10	ms
$t_{o(dom)TXD}$	TXD dominant timeout	RL=60 Ohm, CL open, see Figure 8-5	4	5.5	7	ms
$t_{o(silence)}$	Bus silence timeout	Recessive time	0.9	1	1.17	s
$t_{d(busact-bias)}$	Propagation dela: from active to bias mode				200	µs
$t_{startup(CAN)}$	CAN start-up time	Switch to active (CTS=1)			220	µs
FD TIMING						
$t_{bit(bus)}$	Bit time	STB=0V, bus-side: RL=60 Ohm, CL=100pF, CLrx=15pF, data rate=2Mbps, see Figure 8-6	450		530	ns
$t_{bit(bus)}$	Bit time	STB=0V, bus-side: RL=60 Ohm, CL=100pF, CLrx=15pF, data rate=5Mbps, see Figure 8-6	155		210	ns
$t_{bit(rxd)}$	Bit time	STB=0V, receiver side: RL=60 Ohm, CL=100pF, CLrx=15pF, data rate=2Mbps, see Figure 8-6	400		550	ns
$t_{bit(rxd)}$	Bit time	STB=0V, receiver side: RL=60 Ohm, CL=100pF, CLrx=15pF, data rate=5Mbps, see Figure 8-6	120		220	ns
Δt_{rec}	Receiver timing symmetry	STB=0V, receiver side: RL=60 Ohm, CL=100pF, CLrx=15pF, see Figure 8-6	-65		40	ns
Δt_{rec}	Receiver timing symmetry	STB=0V, receiver side: RL=60 Ohm, CL=100pF, CLrx=15pF, see Figure 8-6	-45		15	ns
BAT, VCC, VIO SUPPLY						
$t_{startup}$	Start-up time	From BAT voltage exceeding power-on detection threshold to INH active		0.8	2	ms
$t_{d(uvd)}$	UVLO detection time	BAT UVLO detection time	6	15	54	µs
$t_{d(uvd-sleep)}$	UVLO to sleep mode delay	VCC and/or VIO UVLO to sleep mode	210	400	490	ms
WAKE TIMING						
t_{wake}	Wake-up time		50			µs
RXD (interrupt or wake-up timing)						
$t_{d(event)}$	Event capture delay time	CAN offline mode	0.9		1.1	ms
t_{blank}	blanking time	From CAN offline to active/listen-only mode		12	25	µs
CAN PARTIAL NETWORKING						
$n_{bit(idle)}$	Number of idle bits	Number of recessive bits before a new SOF shall be accepted; CFDC = 11	6		10	-
$t_{filtr(bit)dom}$	Filter time for dominant bit	Arbitration data rate is less than 500 kbit/s, data bit-rate ≤ 2Mbps, CFDC=1,FD_FL=0	5		17.5	%
		Arbitration data rate is less than 500 kbit/s, data rate ≤ 5Mbps,CFDC=1,FD_FL=1	2.5		8.75	%

Dynamic Characteristics (continued)

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
$t_{cy(clk)}$	SCK clock period	Normal mode/standby mode, see Figure 8-9	250			ns
		Sleep mode	1			µs
$t_{SPILEAD}$	SCSN-fall-to-SCK-rise time	Normal mode/standby mode, see Figure 8-9	50			ns
		Sleep mode	200			ns
t_{SPILAG}	SCK-fall-to-SCSN-rise time	Normal mode/standby mode, see Figure 8-9	50			ns
		Sleep mode	200			ns
$t_{clk(H)}$	SCK pulse width_High	Normal mode/standby mode, see Figure 8-9	100			ns
		Sleep mode	475			ns
$t_{clk(L)}$	SCK pulse width_Low	Normal mode/standby mode, see Figure 8-9	100			ns
		Sleep mode	475			ns
$t_{su(D)}$	SDI input setup time	Normal mode/standby mode, see Figure 8-9	50			ns
		Sleep mode	200			ns
$t_{h(D)}$	SDI input hold time	Normal mode/standby mode, see Figure 8-9	50			ns
		Sleep mode	200			ns
$t_{v(Q)}$	Output data propagation delay	SDO pin, C_L=20pF, normal mode/standby mode, see Figure 8-9			50	ns
		SDO pin, C_L=20pF, sleep mode, see Figure 8-9			200	ns
$t_{d(SDI-SDO)}$	SDI to SDO propagation delay	SCK falling edge-to-SDO valid, C_L=20pF, see Figure 8-9			50	ns
$t_{WH(S)}$	SCSN pulse width_High	SCSN pin, normal mode/standby mode, see Figure 8-9	250			ns
		SCSN pin, sleep mode, see Figure 8-9	1			µs
$t_{d(SCKL-SCSNL)}$	SCK fall to SCSN fall delay time		50			ns

7.7. Typical Characteristics

Over recommended operating conditions, unless otherwise noted.

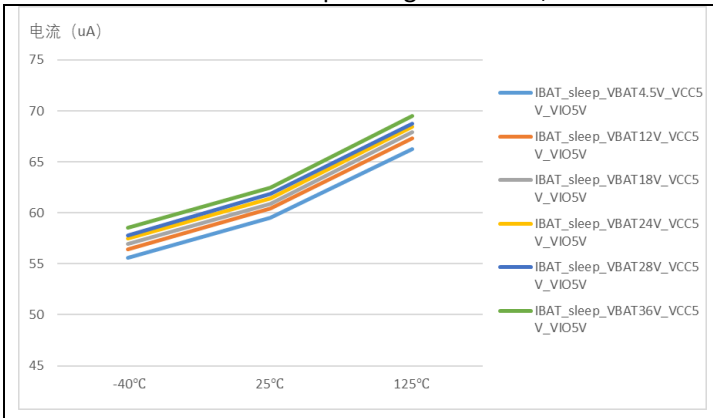


Figure 7-1. Supply current @ listen-only mode

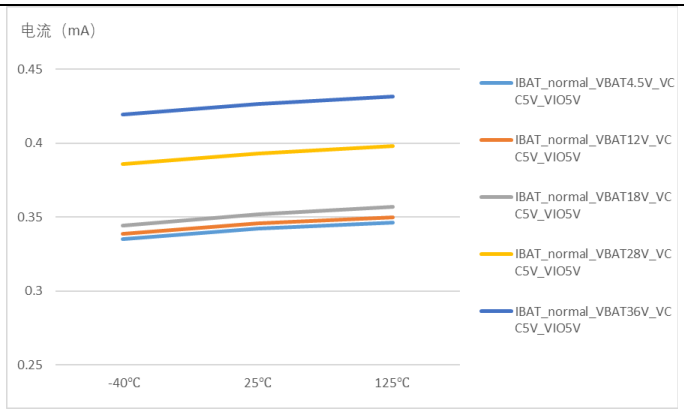


Figure 7-2. Supply current @ recessive state

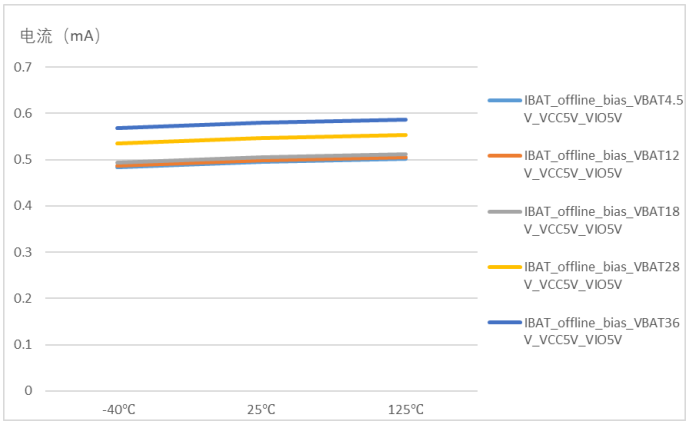


Figure 7-3. Supply current @ offline bias mode

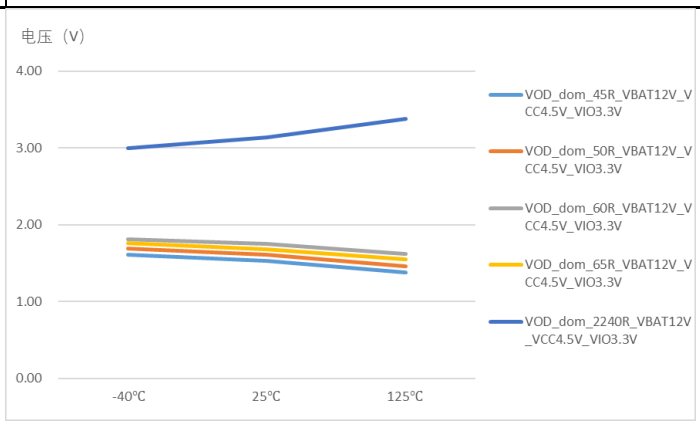


Figure 7-4. Bus output differential voltage (dominant) @ different load

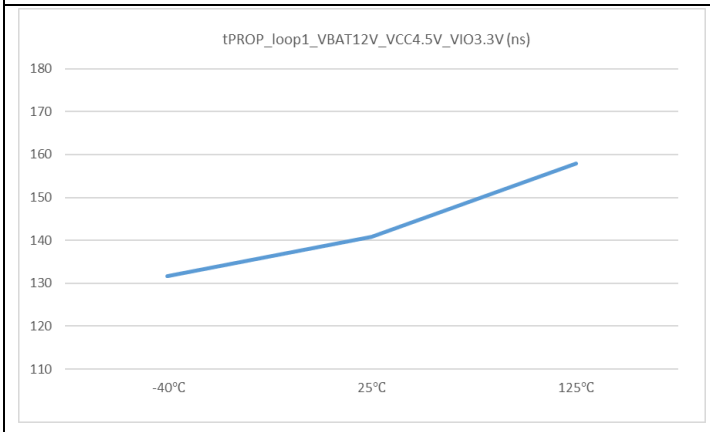


Figure 7-5. Loop delay from recessive to dominant

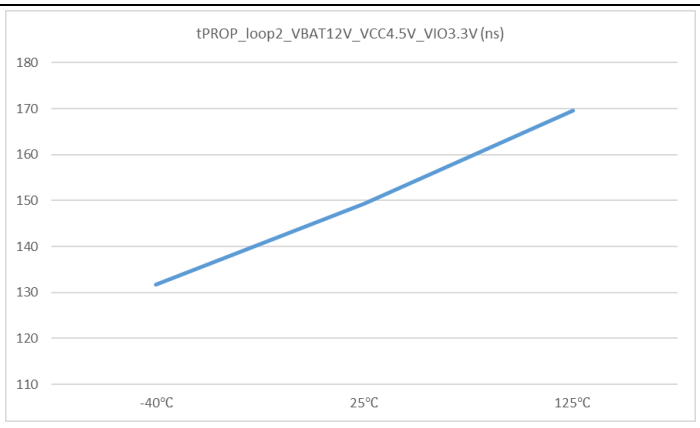


Figure 7-6. Loop delay from dominant to recessive

8. Parameter Measurement Information

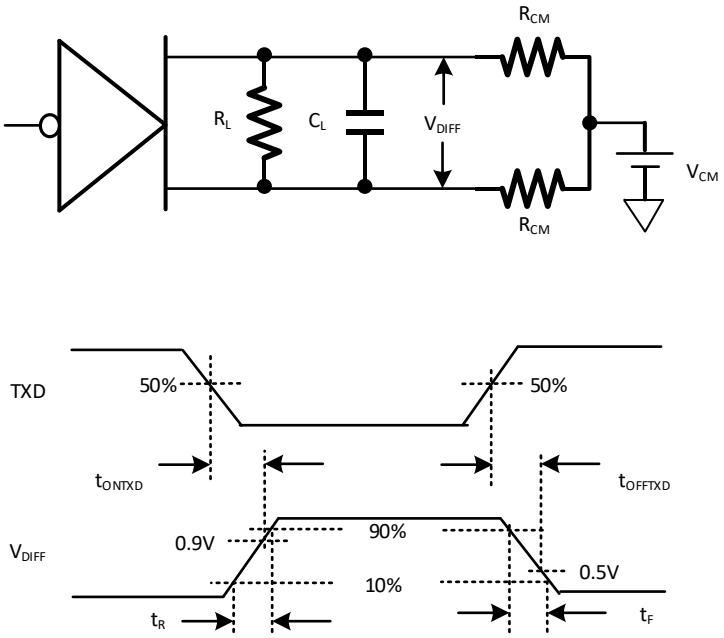


Figure 8-1. Transmitter test circuit and timing diagram

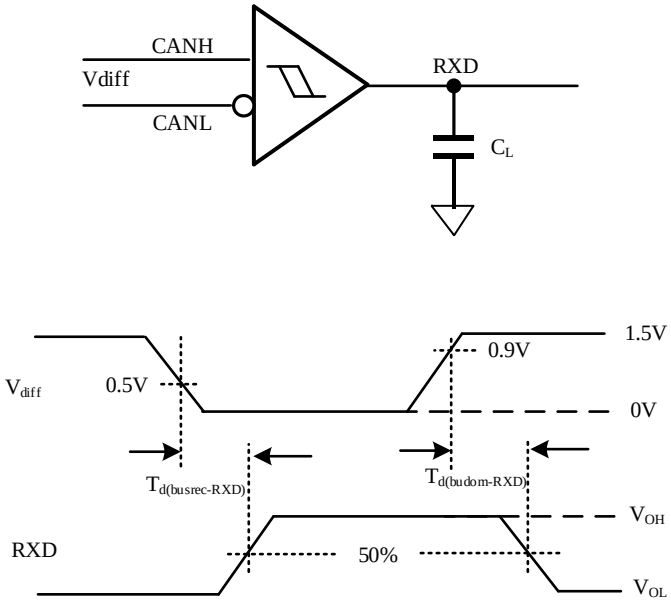


Figure 8-2. Receiver test circuit and timing diagram

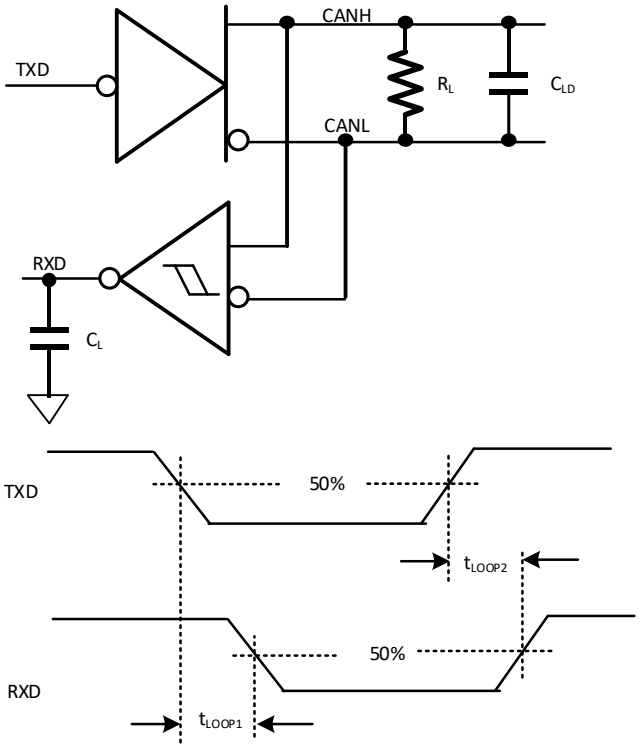


Figure 8-3. TXD to RXD loop delay

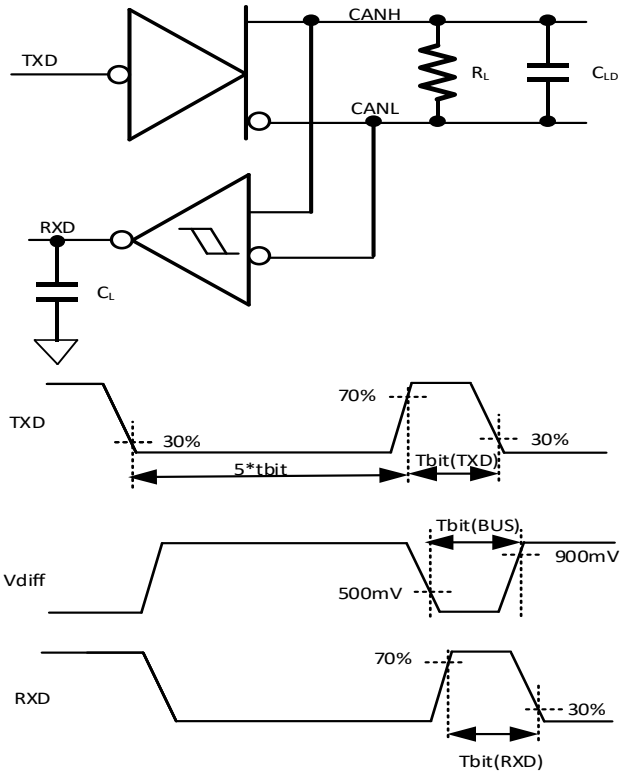


Figure 8-4. FD timing diagram

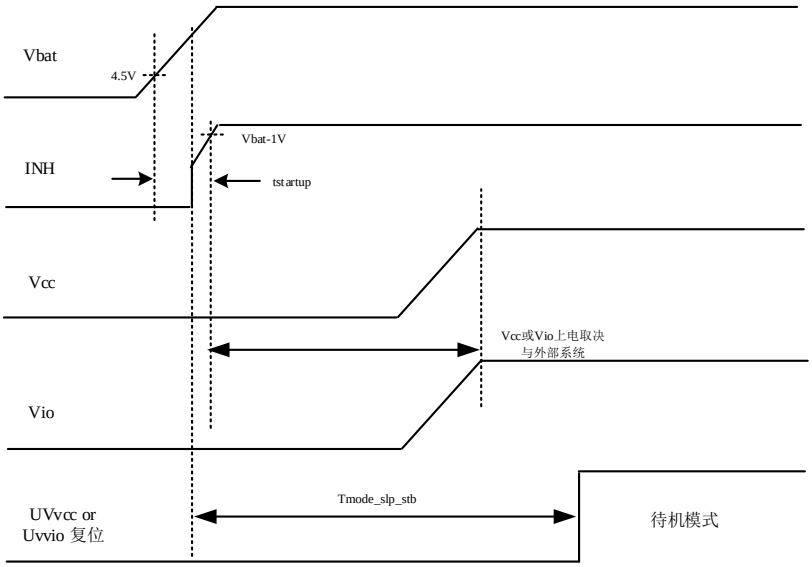


Figure 8-5. Power-on timing diagram

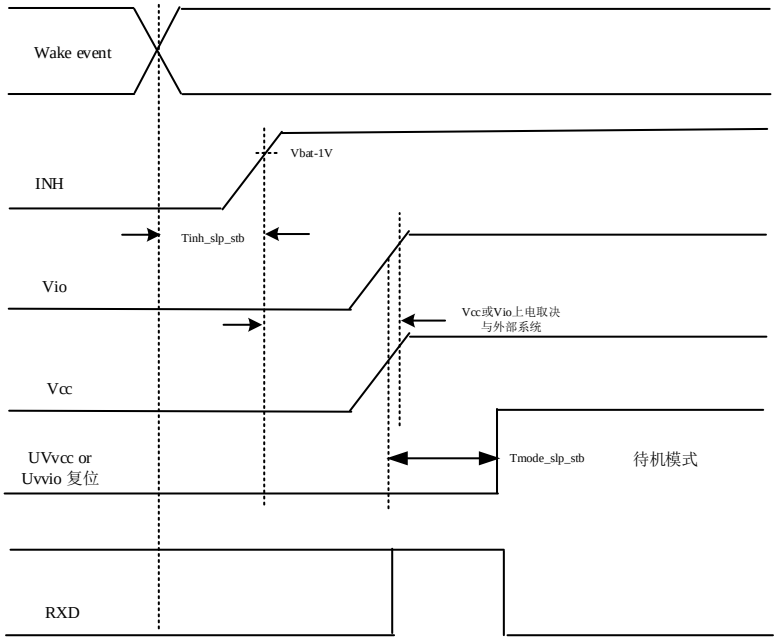


Figure 8-6. Mode change timing diagram: from sleep mode to standby mode

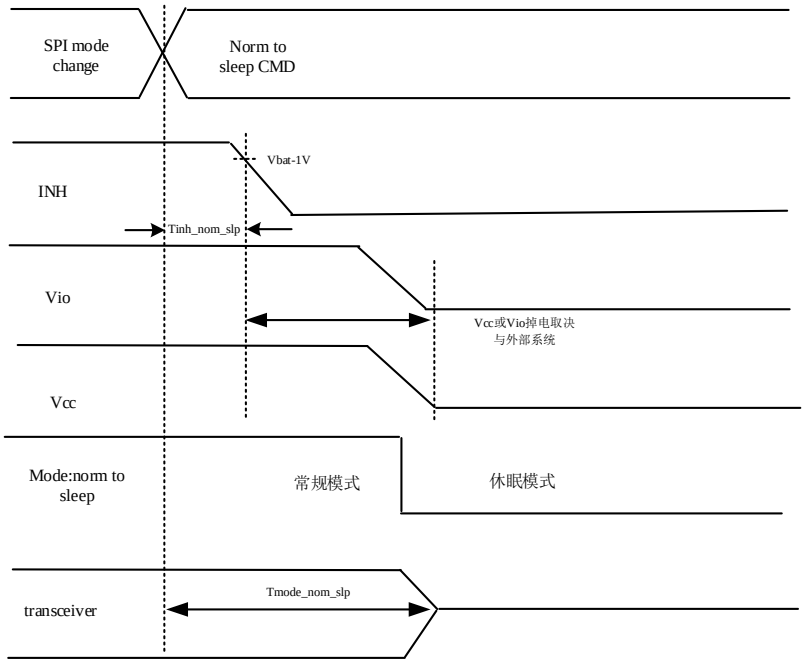


Figure 8-7. Mode change timing diagram: from normal mode to sleep mode

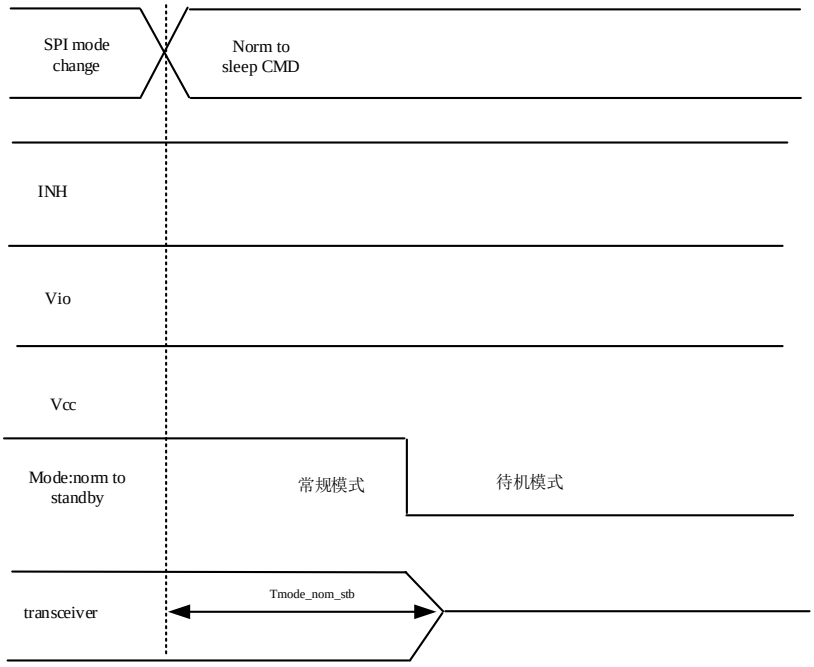


Figure 8-8. Mode change timing diagram: from normal mode to standby mode

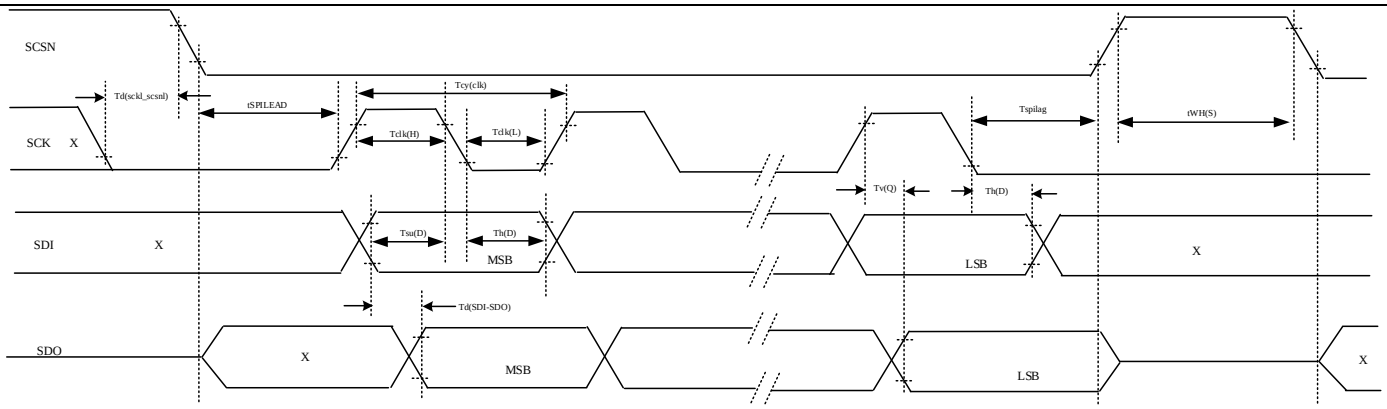


Figure 8-9. SPI timing diagram

9. Detailed Description

9.1. Overview

The CA-IF1145 family of Controller Area Network (CAN) transceivers meets the requirements of ISO11898-2 (2016) and SAE J2284-1 to SAE J2284-5 high-speed CAN physical layer standards, including CAN partial networking support, autonomous bus biasing and advanced power management functions. These devices are designed for automotive applications with a number of integrated robust protection, fail-safe and diagnostic features that improve the reliability of CAN communication. The CA-IS1145 CAN transceivers can operate in low-power modes. A selective wake-up (FD-passive) is able to block CAN FD frames passed through the receiver while waiting for a valid wake-up frame(WUF) in sleep or standby modes to support ISO 11898-2:2016 compliant CAN partial networking and enables reliable communication in the CAN FD (flexible data rate) networks up to 5 Mbit/s data rates.

The functional block diagram of CA-IF1145 is shown in Figure 9-1. The high-speed CAN transceivers in this family are fault protected up to ±42V, and devices communicate with external CAN controllers through a SPI interface and internal controller to configure the registers and control the high-speed CAN transceiver functions. Also, the CA-IF1145 devices feature individual logic supply input (VIO) and provide low level translation to simplify the interface with low voltage CAN controllers.

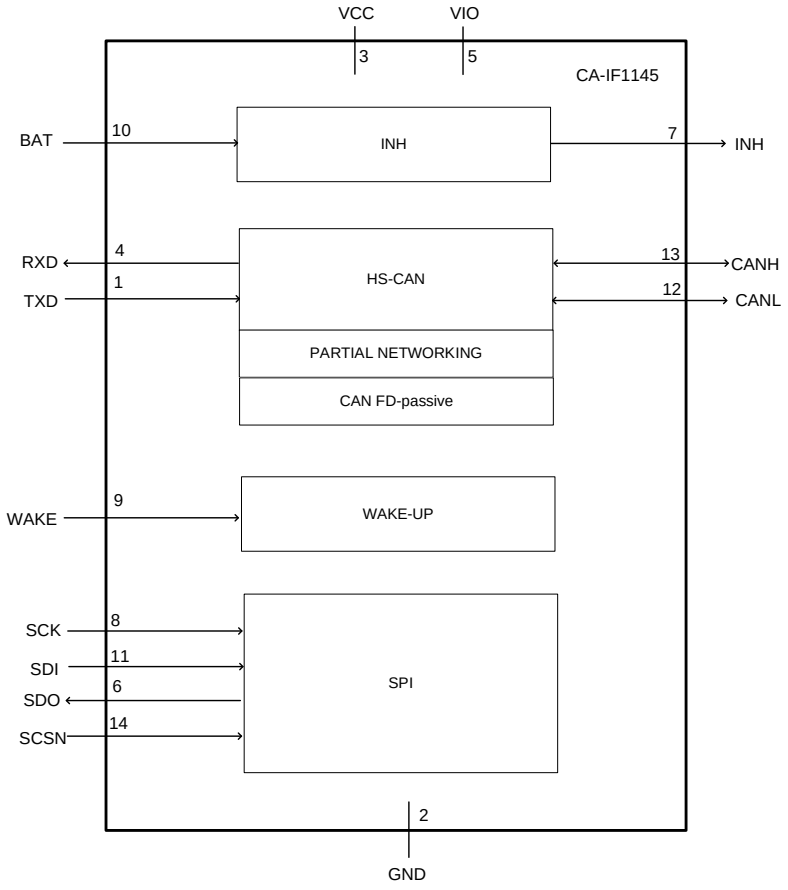


Figure 9-1. Functional block diagram

9.2. Device Operating Modes and Control

The CA-IF1145 internal system controller contains a state machine that supports five operating modes: normal operation mode, standby mode, sleep mode, overtemperature protection mode and off mode, see Figure 9-2. System state diagram and Table 9-1. System operating status1.

9.2.1. Normal Mode

The CAN driver and receiver of the CA-IF1145 can fully operational and CAN communication is bi-directional in normal mode if enabled via CMC configuration. Select normal mode operation from standby or sleep mode by setting MC = 111 (mode control register, 01h) through SPI command, see Table 9-1. INH is logic-high during normal operation, can be used to enable external voltage regulators and microcontroller.

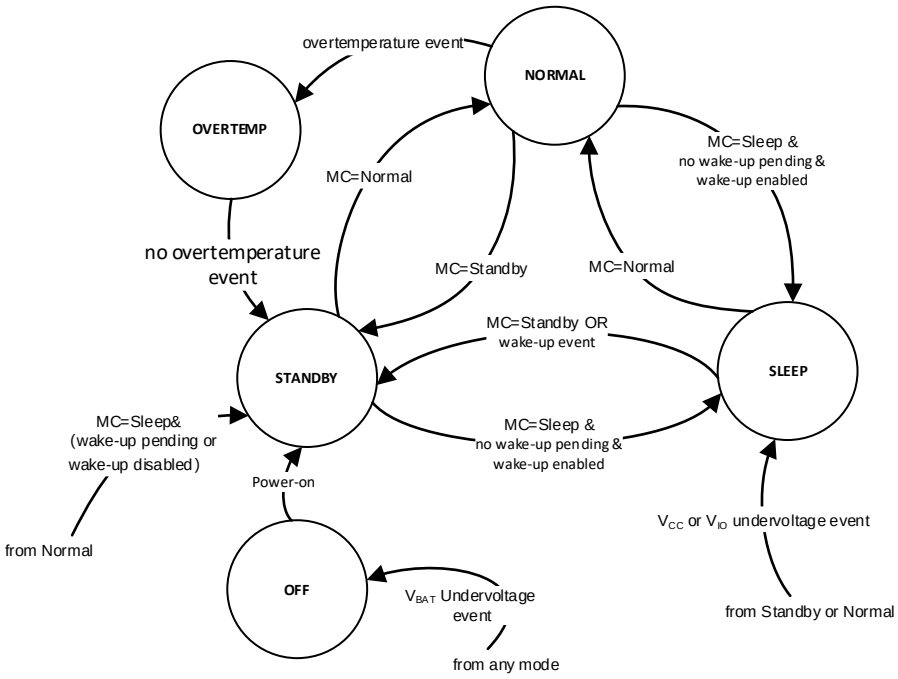


Figure 9-2. System state diagram

Table 9-1. System operating status[1]

Functional Block	Operating Mode				
	Off	Standby	Normal	Sleep	Overtemperature Protection
SPI interface	Disabled	Active	Active	Active if V_{IO} is powered-up [2]	Read only
INH output	Hi-Z	High (V_{BAT})	High (V_{BAT})	Hi-Z	High (V_{BAT})
CAN transceiver	Disabled	Offline	Determined by CMC setup: active/offline/listen-only	Offline	Disabled
RXD output	High (V_{IO})	Low if a remote wake event occurred, otherwise output High.	CAN bit stream if CMC = 01/10/11, otherwise same as standby and sleep modes.	Low if a remote wake event occurred, otherwise output High.	Low if a remote wake event occurred, otherwise output High.

Notes:
1. Hi-Z = high impedance, High = high-level, Low = low-level;
2. SPI communication rate is limited in sleep mode.

9.2.2. Standby Mode

Standby mode is a low-power system operating mode. Both CAN transmitter and receiver are disabled and no communication with the CAN bus in standby mode. In standby mode, the remote wake-up is enabled (CWE = 1, see

Table 9-21), the bus pins are biased to GND when the bus is inactive and the bus bias changes from ground to about 2.5 V while there is activity on the CAN bus and listening for a valid wake-up request. Once a remote wake-up request is detected, RXD will be placed at low-level that can be used as an interrupt for the microcontroller. INH output is on and remains logic-high to enable external voltage regulators. The wakeup sources can be a standard wake-up pattern(WUP) or a selective wake-up frame (CPNC = PNCOK = 1, see Table 9-6. CAN transceiver control register (address = 0x20)).

The CA-IF1145 switches to standby mode in case one of below conditions asserted,

- In off mode, the battery voltage increases and exceeds the BAT power-on detection threshold $V_{th(det)pon}$;
- Under overtemperature protection condition, the device temperature drops below thermal shutdown release threshold $t_{th(rel)otp}$;
- A wake-up request or an interrupt event is detected in sleep mode;
- During normal operation or in sleep mode, the CA-IF1145 receives MC=100 SPI command;
- During normal operation, the CA-IF1145 receives MC = 001 SPI command, while a wake-up request is pending or all wakeup sources are disabled.

9.2.3. Sleep Mode

Sleep mode is the lowest-power operating mode. In sleep mode, the high-speed CAN transmitter and receiver are disabled; INH is turn-off (high impedance) and disable external regulators to reduce battery power consumption; The CAN bus, SPI interface and WAKE pin are continuously monitored for a valid wakeup signal, so that transceiver is able to wakeup by a message on the CAN bus, SPI interface (V_{IO} is powered-up) or local wakeup event through WAKE pin. Whenever a local or remote wake-up, or interrupt event (except SPIF) occurs, the transceiver will enter standby mode automatically which in turn sets the INH output high.

Either or both the V_{CC} or V_{IO} supplies have an undervoltage condition, VCC or VIO voltage drops below the corresponding UVLO threshold and maintained at least $t_{d(uvd)}$, will place the device into sleep mode. In this case, all of pending wake-up requests will be cleared, selective wake-up is disabled (CPNC = 0), CAN bus wake-up (CWE = 1) and local wake-up (WPFE = WPRE = 1) detection are enabled to avoid system deadlock, see

Table 9-21and Table 9-22.

During normal operation or standby mode, the CA-IF1145 switches to sleep mode through MC = 001 SPI command in case of there are no pending wake-up events and at least one regular wake-up source (see Regular Wake-up Events section) is enabled. It is important to configure the event detection correctly when the CA-IF1145 switches to sleep mode. To avoid potential system deadlocks, at least one regular wake-up event must be enabled and all event status bits must be cleared before the CA-IF1145 switches to sleep mode. After the CA-IF1145 enters sleep mode, if SPI command disable all of wake-up sources, the device will switch to standby mode automatically to avoid system deadlock.

The sleep mode switching status flag (FSMS) in the main status register, 0x03 (see Table 9-3) is set either high or low to identify whether a transition to sleep mode was selected via an SPI command or was forced by an undervoltage event on VCC or VIO pins:

- FSMS = 0 means that the sleep mode was selected through SPI command;
- FSMS = 1 means that the sleep mode was occurred by an UVLO event on VCC or/and VIO pins.

This FSMS flag bit can be read through SPI interface after the device is returned to normal operation or standby mode, then setup CWE, WPFE, WPRE and CPNC status as needed.

9.2.4. Off Mode

When the voltage on BAT pin drops below power-off threshold $V_{th(det)poff}$ for longer than $t_{d(uvd)}$, the device is put into off mode. Both CAN transmitter and receiver are disabled, leave the bus pins and RXD in high-impedance. INH goes high impedance to disable external voltage regulators as needed. Off mode is the power-on default device status when the battery supply is first applied on BAT input. When the battery supply voltage increases above the power-on threshold $V_{th(det)pon}$, the CA-IF1145 starts an initialization procedure, then switches to standby mode after $t_{startup}$.

9.2.5. Overtemperature Protection Mode

Once the device junction temperature exceeds thermal shutdown threshold $T_{th(act)otp}$ (190°C, typ), will put the CA-IF1145 into overtemperature protection mode immediately, turn off the CAN transmitter thus blocking the TXD-to-bus transmission path. Also CAN receiver is disabled and can not detect wakeup events, but a pending wake-up event will still place RXD to low level, and RXD pin will keep low after the overtemperature condition cleared. The shutdown condition is cleared and the CA-IF1145 switches to standby mode when the junction temperature drops at least the thermal shutdown hysteresis temperature below the thermal shutdown threshold, or the device is put into off mode if the battery voltage is lower than $V_{th(det)poff}$. INH remains logic-high during thermal shutdown.

To prevent data losing due to overheating, the CA-IF1145 issues an alarm signal when the device junction temperature rises above the overtemperature warning threshold $T_{th(warn)otp}$ (140°C, typ). When the threshold $T_{th(warn)otp}$ is reached, the overtemperature alarm status bit OTWS is set and an overtemperature interrupt is triggered (OTW = 1) if OTWE = 1 (overtemperature alarm enable control bit, see Table 9-20).

9.2.6. Device System Control Register

The external CAN controller can write to the mode control register (address = 0x01) via SPI interface to setup system operating modes, see Table 9-2. The main status register(address = 0x03) can be accessed to monitor the overtemperature warning flag and whether the CA-IF1145 has entered normal mode after power-up. It also indicates the source of latest events, such as, the transition to sleep mode was triggered by V_{CC} or V_{IO} undervoltage event or by an SPI command, see Table 9-3.

Table 9-2. Mode control register (address = 0x01)

Bit	Symbol	Type[1]	Value	Description
7:3	Reserved	R	-	
2:0	MC	R/W		Mode control
			001	Sleep mode
			100	Standby mode
			111	Normal mode

Note:
1. R: Read only; R/W: Read and Write; X: Don't care.

Table 9-3. Main status register (address = 0x03)

Bit	Symbol	Type[1]	Value	Description
7	FSMS	R	-	Sleep mode switching status
			0	Device enters sleep mode through SPI command.
			1	VCC or VIO UVLO event put device into sleep mode.
6	OTWS	R		Overtemperature alarm status
			0	Junction temperature < $T_{th(warn)otp}$
			1	Junction temperature ≥ $T_{th(warn)otp}$

5	NMS	R		Normal operation status
			0	Device has entered normal mode after power-up.
			1	Device has powered up but didn't go to normal mode.
4:0	Reserved	R	-	

9.3. Fail-safe and Protection Functions

The CA-IF1145 provides robust high-speed CAN transceiver with overvoltage fault protection, over-current protection, under-voltage lockout during all modes of operation. Also, the local and remote bus failures detection can prevent damage to the device or interference with CAN bus communication, that benefits the troubleshooting in a CAN bus system and improves equipment operating efficiencies.

9.3.1. Overvoltage Fault Protection

The CA-IF1145 devices has an internal ±42V overvoltage protection circuit on the transmitter output and receiver input to protect the devices from accidental shorts between a local power supply and the data lines of the transceivers. This level of protection is present whether the transceiver is powered or un-powered. Also, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly.

9.3.2. Current-Limit

The CA-IF1145 protects the transmitter output stage against a short-circuit to a positive or negative voltage by limiting the driver current. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. Also, the device has transmitter dominant timeout detection which prevents permanently having the higher short circuit current of dominant state in case of a system fault.

9.3.3. Floating Terminals

The CA-IF1145 devices have internal pull-up or pull-down on critical terminals to place the device into known states if the terminals float. The TXD terminal is pulled up to VIO to force a recessive input level if the terminal floats.

9.3.4. Undervoltage Lockout

The CA-IF1145 has undervoltage detection on VCC, VIO and BAT supply terminals that place the device into low-power mode or protected mode during an undervoltage event. When the voltage on BAT pin drops below power-off threshold $V_{th(det)poff}$ for longer than $t_{d(uvd)}$, the device switches off mode. Battery supply losing at pin BAT will not affect CAN bus or the microcontroller operation because no reverse current will flow from the bus. Once V_{BAT} under voltage condition is cleared and the battery supply returned to valid level, above the power-on threshold $V_{th(det)pon}$, the CA-IF1145 starts an initialization procedure, then switches to standby mode after $t_{startup}$.

When CMC = 01 and VCC voltage drops below $V_{UVD(VCC)}$, a CAN failure interrupt will be generated (CF = 1) if CAN failure detection is enabled (CFE = 1) and VCC supply voltage status bit VCS is set. Either or both the V_{CC} or V_{IO} supplies have an undervoltage condition, VCC or VIO voltage drops below the corresponding UVLO threshold and maintains at least $t_{d(uvd)}$, the CA-IF1145 device will go to sleep mode. As mentioned in Sleep Mode section, when the CA-IF1145 is forced to sleep mode, it is important to configure the device according to below items to ensure that the device will respond to a wake-up event and avoid potential system deadlocks:

- Clear all of captured events previously (address 0x61 -- 0x64) before the CA1145 switches to sleep mode to avoid repeated wake-up under VCC/VIO undervoltage conditions.
- CAN bus wake-up (CWE = 1) and local wake-up (WPFE = WPRE = 1) detection are enabled, to ensure that the CA-IF1145 is able to be woken after switching into sleep mode;

- The selective wake-up is disabled (CPNC = 0), thus the CA-IF1145 is able to be woken once the device recovered from undervoltage events;
- Clear the partial networking configuration (CPNOK=0), CAN partial networking may not be configured correctly when the CA-IF1145 goes into sleep mode.

The sleep mode switching status flag (FSMS) is set when an undervoltage event occurred and put the device into sleep mode. FSMS bit can be read out through SPI interface after the device return to normal mode or standby mode, then setup CWE, WPFE, WPRE and CPNC status as needed.

If the CA-IF1145 switches to sleep mode because of undervoltage events, the device will switch to standby mode to respond MC = 001 or MC = 111 SPI command after the undervoltage condition is cleared on VIO and the supply voltage has returned to a valid level, the UVLO counter is reset to zero.

9.3.5. Transmitter-Dominant Timeout

The CA-IF1145 devices feature a transmitter-dominant timeout ($t_{o(dom)TXD}$) detection that prevents erroneous CAN controllers from clamping the bus to a dominant level by maintaining a continuous low TXD signal. When TXD remains in the dominant state (low) for greater than $t_{o(dom)TXD}$, the transmitter is disabled, releasing the bus to a recessive state. A CAN failure interrupt is generated (CF = 1), if CFE = 1; In addition, the status of the transmitter dominant timeout can be read by CFS bit in the transceiver status register and CTS bit is set to 0.

After a dominant timeout fault, the transmitter is re-enabled and dominant timeout timer is reset when receiving a rising edge at TXD input. The transmitter-dominant timeout limits the minimum possible data rate.

9.4. High-speed CAN Transceiver

The CA-IF1145 high-speed CAN transceiver support low-power operation mode, as well as wake-up capability over CAN bus, or via the WAKE pin, SPI command. Inhibit output (INH) can be used to control one or more external voltage regulators presented on a node to reduce the battery power consumption at system level. Also, the CA-IF1145 features CAN FD-passive by a dedicated implementation of the partial networking protocol.

9.4.1. Receiver

The receiver of CA-IF1145 supports normal bi-directional communication and the bus line wakeup event detection. In normal operation and the transceiver is active, the receiver reads the differential input from the bus line (CANH and CANL) and transfers this data as a single-ended output RXD to the CAN controller. The internal comparator senses the difference voltage V_{DIFF} = (V_{CANH}-V_{CANL}), with respect to an internal threshold of 0.7V. If V_{DIFF} > 0.9V, a logic-low is present on RXD; If V_{DIFF} < 0.5V, a logic-high is present. Table 9-4 shows the receiver truth table.

Table 9-4. Receiver truth table

DEVICE MODE	V_{ID} = V_{CANH}-V_{CANL}	BUS STATE	RXD
Active/listen-only CMC = 01/10/11	V_{ID} ≥ 0.9V	Dominant	Low
	0.5V < V_{ID} <0.9V	Indeterminate	Indeterminate
	V_{ID} ≤ 0.5V	Recessive	High
	Open (V_{ID} ≈ 0V)	Open	High
Standby Sleep	V_{ID} > 1.15V	Dominant	Low if a remote wake event occurred, otherwise output High.
	0.4V < V_{ID} <1.15V	Indeterminate	
	V_{ID} ≤ 0.4V	Recessive	
	Open (V_{ID} ≈ 0V)	Open	

Note:
X = Don't care

As mentioned in Device Operating Modes and Control section, the CA-IF1145 can be configured into low-power operation modes: standby mode and sleep mode. In standby and sleep modes, both CAN transmitter and receiver are disabled and bidirectional CAN communication is not possible, but the CAN bus, SPI interface and WAKE pin are continuously monitored for a valid wakeup signal. RXD is logic high until a valid wakeup signal is received.

9.4.2. Transmitter

In normal operation, if the transceiver is active, the transmitter converts a single-ended input signal (TXD) from the local CAN controller to differential outputs for the bus lines CANH and CANL. The truth table for the transmitter is provided in Table 9-5. The CA-IF1145 protects the transmitter output stage against a short-circuit to a positive or negative voltage by limiting the driver current. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. The transmitter returns to normal operation once the junction temperature drops at least the thermal shutdown hysteresis temperature below the thermal shutdown temperature. In standby and sleep modes, the transmitter is disabled and put the bus in high-impedance with internal weak pull-down to ground.

Table 9-5. Transmitter truth table (when not connected to the bus)

DEVICE MODE	TXD INPUT	TXD LOW TIME	OUTPUT		BUS STATE
			CANH	CANL	
Normal CMC=01 or 10	Low	< $t_{o(dom)TXD}$	High	Low	Dominant
	Low	> $t_{o(dom)TXD}$	V_{CC}/2	V_{CC}/2	Recessive
	High or Open	X	V_{CC}/2	V_{CC}/2	Recessive
Listen-only CMC = 11	X	X	High-Z	High-Z	Biased to 2.5V
Standby	X	X	High-Z	High-Z	Weakly biased to GND
Sleep	X	X	High-Z	High-Z	Weakly biased to GND
Note: X = Don't care					

9.4.3. CAN Operating Modes

The high-speed CAN transceiver of CA-IF1145 can operate in four modes: active mode, listen-only mode, offline mode, offline bias mode. The transceiver operating mode is determined by the bus status and internal state machine controller, see Figure 9-3. CAN transceiver state diagram.

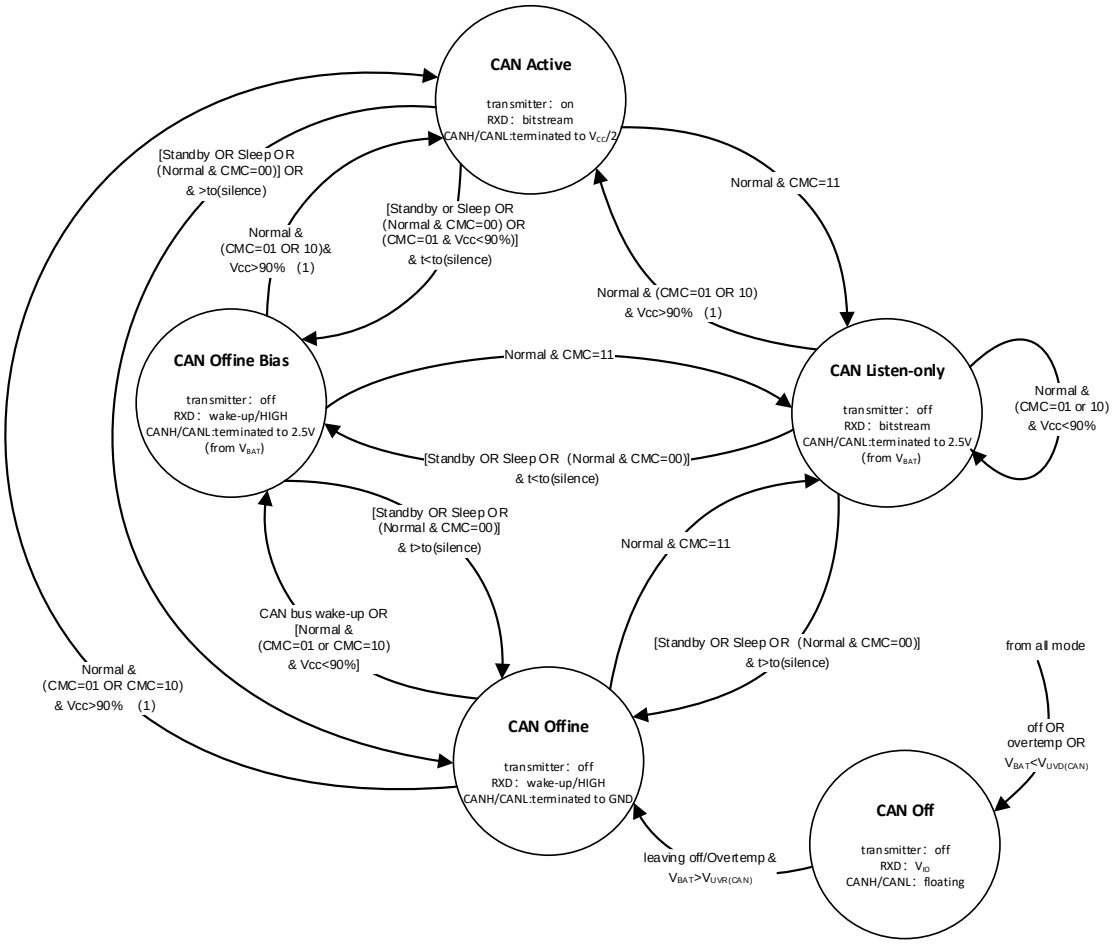
These devices feature autonomous bus biasing to minimize RF emissions. The CA-IF1145 biases the CAN bus (CANH/CANL) to 2.5V when the transceiver is in active mode or listen-only mode (CMC=01/10/11); If there is activity on the bus, or if other nodes are communicating, the CAN bus will stay biased to 2.5V (CAN offline bias mode); If there is no activity on the bus for t > $t_{to(silence)}$, the CAN bus will be biased to ground (CAN offline mode). Autonomous biasing ensures that the CAN bus is correctly biased to avoid disturbing normal communication between other CAN nodes. The autonomous CAN bias voltage is derived from battery supply directly.

CAN Active Mode

In active mode, the CAN transceiver supports bidirectional bus communication and CAN bus is biased to V_{CC}/2 @ recessive state, the CAN bias voltage is derived from VCC supply. In normal operation, if CMC = 01 or 10, the CAN transceiver enters active mode. The VCC UVLO detection is enabled when CMC = 01 and put CAN transceiver into offline/offline bias mode once the V_{CC} supply voltage drops below UVLO threshold $V_{UVD(CAN)}$; The VCC UVLO detection is disabled when CMC = 10, the CAN transceiver will remain active until the device is forced into sleep mode because of V_{CC} supply voltage drops below VCC

UVLO threshold $V_{UVD(VCC)}$, then the transceiver enters offline/offline bias mode.

In normal operation (MC = 111), select CAN transceiver active mode by setting CMC = 10 or 01 and $V_{CC} > V_{UVD(CAN)}$. If the TXD remains in the dominant state (low level), CAN transceiver will switch to listen-only or remain listen-only mode until TXD goes to high-level. This allows other nodes to communicate to prevent bus lockup caused by controller error or by a fault on the TXD input. Reading the CAN transceiver status bit (CTS, see Table 9-7), external CAN controller can determine whether the CAN transceiver is ready for data transmission.



Note（1）: CAN transceiver can not enter active mode when TXD is pulled to GND.

Figure 9-3. CAN transceiver state diagram

CAN Listen-only Mode

Select CAN listen-only mode from normal operation by setting CMC = 11 through SPI interface. In listen-only mode, CAN transmitter is disabled and receiver keeps normal operation, CAN bus is biased at 2.5V if bus active. Also, CAN transceiver will stay at listen-only mode when the TXD remains low-level state, or V_{CC} voltage is lower than UVLO threshold $V_{UVD(VCC)}$ when CMC = 01 or 10.

CAN Offline Mode/Offline Bias Mod

The only difference between CAN offline bias mode and CAN offline mode is that CAN bus is biased at 2.5V in offline bias mode and CAN bus is weakly biased to GND in offline mode. In CAN offline mode, the transceiver monitors the CAN bus for a wake-up event if CAN wake-up detection is enabled (CWE = 1). CAN offline bias mode activated automatically when activity is detected on bus while the transceiver is in CAN offline mode. The transceiver will return to CAN offline mode if the CAN bus is

silent for longer than $t_{to(silence)}$.

The CAN transceiver switches to offline/offline bias mode from active mode if CMC = 01 and the VCC supply voltage drops below UVLO threshold $V_{UVD(VCC)}$, or if CMC = 10 and device goes to sleep mode because of VCC supply voltage drops below $V_{UVD(VCC)}$.

The CAN transceiver switches to offline mode from active or listen-only mode if the CA-IF1145 device goes to standby/sleep mode, or the device is in normal mode but CMC = 00. The CAN transceiver will enter offline bias mode first or offline mode directly based on whether the bus is active or has been inactive at least $t_{to(silence)}$; If CAN bus is active, transceiver switches to offline bias mode first, then goes to CAN offline mode once the bus has been silent for $t_{to(silence)}$.

The CAN transceiver switches to CAN offline mode from CAN offline bias mode if no activity is detected on bus for t > $t_{to(silence)}$ or when device switches from off/overtemperature protection mode to standby mode. In CAN offline mode, if wake-up detection is enabled (CWE = 1), CAN receiver will monitor CAN bus status and wait for a wake-up event. Once a standard wake-up pattern(WUP) is detected on the CAN bus, the CAN transceiver switches from CAN offline mode to CAN offline bias mode. This autonomous CAN biasing ensures CANH and CANL are always biased to a correct level and allow other nodes on the bus to communicate correctly. V_{BAT} provides supply voltage for the autonomous CAN bias circuit.

CAN Off Mode

When the CA-IF1145 device switches to off mode or overtemperature protection mode, or when the battery voltage (V_{BAT}) drops below CAN bus UVLO detection threshold $V_{UVD(CAN)}$, both CAN transmitter and receiver are fully disabled and leave the bus float. This mode prevents reverse currents flowing from CAN bus when battery supply power-off. When BAT voltage rises above the undervoltage recovery threshold $V_{uvr(CAN)}$, the CAN transceiver will switch to offline mode from off mode or overtemperature protection mode.

9.4.4. CAN Transceiver Control Register and Status Register

Table 9-6. CAN transceiver control register (address = 0x20)

Bit	Symbol	Type[1]	Value	Description
7	Reserved	R	-	
6	CFDC	R/W		CAN FD tolerance
			0	Disable CAN FD tolerance
			1	Enable CAN FD tolerance
5	PNCOK	R/W		CAN partial networking configuration
			0	Partial networking register configuration error (standard wake-up pattern only)
			1	Partial networking registers configured correct
4	CPNC	R/W		Selective wake-up configuration
			0	Disable the selective wake-up
			1	Enable the selective wake-up
3:2	Reserved	R	-	
1:0	CMC	R/W		CAN transceiver operating mode selection
			00	Offline mode
			01	Active mode (normal operation); VCC UVLO detection is enabled.
			10	Active mode (normal operation); VCC UVLO detection is disabled.
			11	Silent mode

Note:
1. R: Read only; R/W: Read and Write; X: Don't care.

Table 9-7. CAN transceiver status register (address = 0x22)

Bit	Symbol	Type[2]	Value	Description
7	CTS	R		CAN transceiver status
			0	not in active mode
			1	active mode
6	CPNERR	R		CAN partial networking error status
			0	no CAN partial networking error (PNFDE=0 and PNCOK=1)
			1	Detected CAN partial networking error (PNFDE=1 or PNCOK=0), device can be woken via standard wake-up signal only.
5	CPNS	R		CAN partial networking configuration status
			0	CAN partial networking configuration error (PNCOK=0)
			1	CAN partial networking configuration is correct (PNCOK=1)
4	COSCS	R		CAN oscillator status
			0	CAN partial networking oscillator running at incorrect frequency
			1	CAN partial networking oscillator running at correct frequency
3	CBSS	R		CAN bus is silent
			0	CAN bus is active
			1	CAN bus remains inactive longer than $t_{to(silence)}$
2	Reserved	R		
1	VCS [1]	R		VCC supply voltage status
			0	$V_{CC} > V_{uvd(vcc)}$
			1	$V_{CC} < V_{uvd(vcc)}$
0	CFS	R		CAN bus failure
			0	no transmitter dominant timeout
			1	Detected transmitter dominant timeout, disable CAN transmitter

Notes:
1. Active only when CMC = 01 and device is in normal mode;
2. R: Read only; R/W: Read and Write; X: Don't care.

9.5. Wake-up Events

9.5.1. Regular Wake-up Events

Advanced power management and wake-up capability make the CA-IF1145 ideal for the battery power applications. The CA-IF1145 has two regular ways to exit sleep mode:

- Standard remote wake-up **(**CWE = 1)**:** remote CAN wake-up is enabled (CWE = 1), but CAN selective wake-up is disabled (CPNC = 0 or PNCOK = 0)
- Local wake-up: state change on WAKE terminal.

Standard Remote Wake-up

If standard remote wake-up detection is enabled (CWE = 1) and selective wake-up is disabled (CPNC = 0 or PNCOK = 0), the CA-IF1145 CAN receiver will monitor CAN bus status and wait for a wake-up pattern(WUP) in offline mode. To improve the system operation reliability and prevent false wake-up, the CA-IF1145 receiver features wakeup timeout detection and filtered CAN bus status wakeup detection according to the ISO 11898-2:2016 standard. This means, for a valid dominant and recessive

status to be considered, the bus must be kept in that state for more than the $t_{wake(busdom)}$ or $t_{wake(busrec)}$ respectively. For a standard remote wake-up event to successfully occur, a dominant bus level greater than $t_{wake(busdom)}$ must be detected and received by the receive channel first to initiate a wake-up event detection; Then the monitor will wait for a valid recessive state (a recessive phase of at least $t_{wake(busrec)}$) from CAN bus. Once a valid recessive pulse is received, the bus monitor is waiting for the 2nd valid dominant state, other bus traffic does not reset the bus monitor. Once the receive channel detects a successful wake-up event (a series of valid dominant - recessive - dominant pulses) within the timeout value $t \le t_{to(wake)bus}$, RXD pulls low and INH pulls high, the wake-up bit CW in the transceiver event status register(0x63) is set. RXD is high until a valid wake-up pattern is received in sleep mode, see Figure for more details.

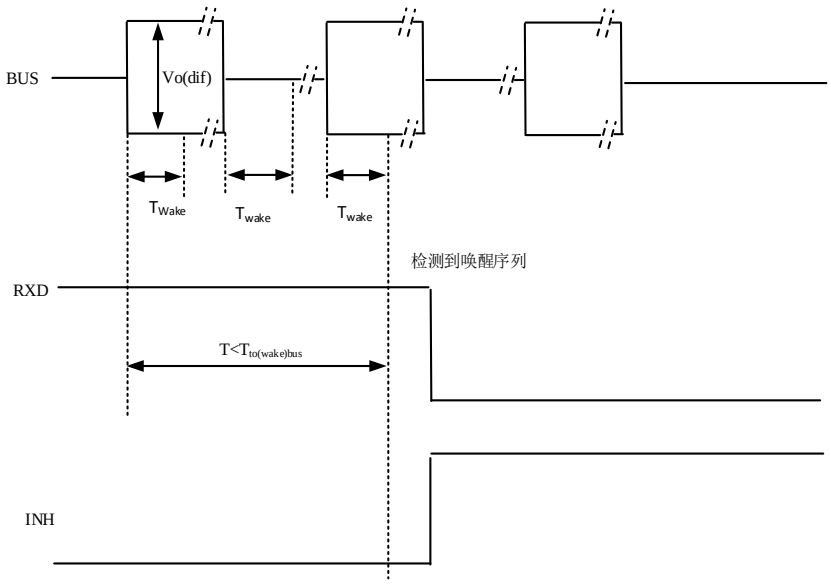


Figure 9-4. Standard remote wake-up

Local Wake-Up

A valid local wake-up request is generated either a low to high rising edge (WPRE = 1), or a high to low falling edge (WPFE = 1) transition on WAKE terminal. The WAKE is a high voltage input terminal. The local wakeup request is active in normal, standby and sleep modes. For the unused local wakeup design, it is recommended to connect pin WAKE to GND to prevent EMI issues. While in normal mode, the CA-IF1145 is able to monitor the status of pin WAKE by reading WPVS bit, see Table 9-8. Otherwise, WPVS is only valid when local wake-up is enabled (WPRE = 1 and/or WPFE = 1).

Table 9-8. WAKE status register (address = 0x4B)

Bit	Symbol	Type[1]	Value	Description
7:2	Reserved	R	-	
1	WPVS	R		WAKE pin status
			0	WAKE voltage below switching threshold ($V_{th(sw)}$)
			1	WAKE voltage above switching threshold ($V_{th(sw)}$)
0	Reserved	R	-	
Note: R: Read only; R/W: Read and Write; X: Don't care.				

9.5.2. Selective Wake-up

The CA-IF1145 supports selective wake-up according to ISO 11898-2:2016 that can be used to enable the nodes as needed only in a CAN networking. When selective wake is enabled, only the specific or desired wake-up frame (WUF) can wake the device, unless there is some type of error threshold that is hit (such as a decoding error). The selective WUF is based on

the CAN frame defined in ISO 11898-1:2015 standard, consisting of identifier field (ID), data length code (DLC), data field and CRC (cyclic redundancy check) code with CRC delimiter. The CA-IF1145 has selective wake control registers to setup the device to detect a programmed match using either the CAN ID, or the CAN ID plus the data frame including data masking. The CAN ID can be a standard (11-bit) format or extended (29-bit) format that is selected by IDE bit in the frame control register (2Fh), see Table 9-12.

A valid WUF identifier is stored in the partial networking ID registers (Table 9-10). The ID mask register (Table 9-11) defines a group of valid identifiers to be detected by individual CAN node, where “1” means ‘do not care’ the corresponding identifier bit. For example, a standard frame shown in Figure 9-5, the 11-bit identifier is defined as 0x1A0 reserved in ID registers 0x29 and 0x2A. The three least significant bits of the ID mask are set to 1, which means that the corresponding identifier bits 2 to 0 are ‘do not care’. This means any of eight different identifiers from 0x1A0 to 0x1A7 will be recognized as valid wake in the received WUF.

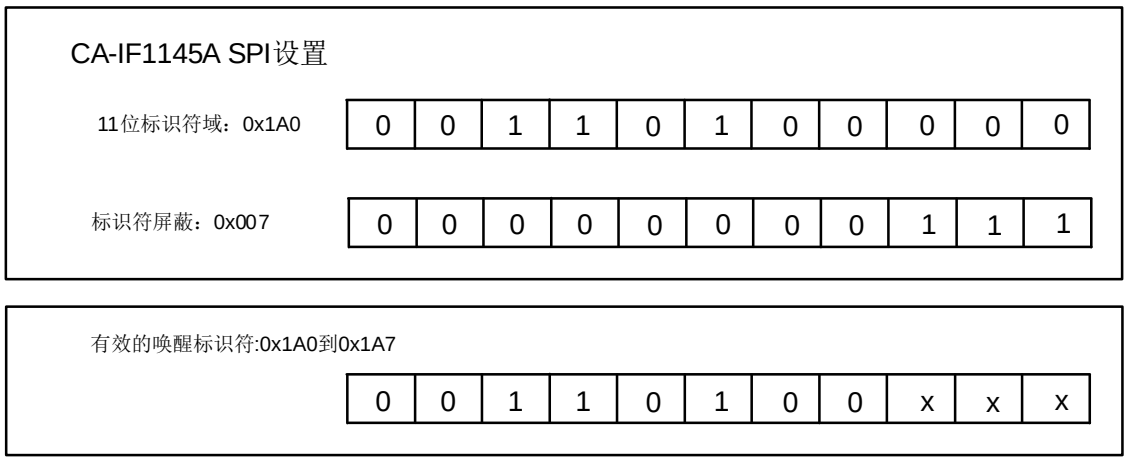


Figure 9-5. Identifier field detection in a selective WUF

The data field defines which CAN nodes to be woken up. The CA-IF1145 compares the incoming data field with the data mask bits (Table 9-13). A single wake-up message can wake-up multiple nodes simultaneously. The data length code (DLC) in the frame control register (Table 9-12) defines the number of data bytes in WUF data field, 0 to 8 bytes. If DLC ≠ 0000, for a successful wake-up, at least one bit in the data field of the received wake-up frame must be set to 1 and at least one equivalent bit in the associated data mask register (68h to 6Fh, Table 9-13) must also be set to 1. Each pair of matched “1” indicates a group of nodes to be woken-up, since the data field length is up to 8 byes, there are up to 64 groups of nodes can be defined. If DLC ≠ 0000 and all data mask bits are set to 0, the device cannot be woken up by CAN bus, note that all data mask bits are default “1”.

If DLC = 0000, a CAN node will wake up if the WUF contains a valid ID and the received data length code is 0000, regardless of the values stored in the data mask. If a WUF contains a valid ID but the DLC in the WUF and the DLC in the frame control register are not matched, the data field will be ignored and there are no CAN nodes wake-up occurred. Figure 9-6 shows an example for valid WUF data field detection, DLC = 1, the data field is a single byte; This means that device will compare the incoming data filed of WUF with data mask 7 (DM7 in the data mask registers 6Fh). In this example, DM7 = 10101000 and up to three groups of nodes could be woken up (group 1, 3 and 5) if the respective bits in the data frame are also set to 1. In Figure 9-6, the received message could wake up four groups of nodes potentially: groups 2, 3, 4 and 5; As there are two matched bits found (groups 3 and 5) when the message data bits are compared with DM7, group 3 and group 5 can be woken-up.

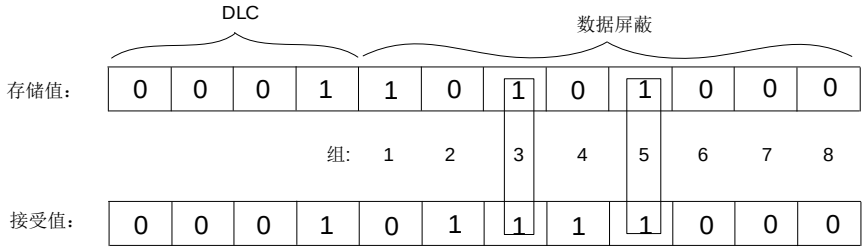


Figure 9-6. Data field detection in a selective wake-up frame

DLC and data filed are optional in the wake-up filtering. If PNDM = 0, the data length code and data field will be ignored in the wake-up message evaluation; If PNDM = 1(default), the data field will be included in the wake-up message evaluation.

If PNDM = 0, when the following conditions are met, the received frame shall be a valid wake-up frame and CAN wake-up flag (CW) will be set to 1 (CW = 1):

- The identifier field of received WUF is exactly matching the configured pattern in the ID register after filtering, AND
- A CRC field has been received, including a recessive CRC delimiter, and no error is detected prior to the acknowledgment(ACK) slot.

If PNDM = 1, a valid wake-up frame is captured and CAN wake-up flag (CW) will be set to 1 when:

- The identifier field of received WUF is exactly matching the configured pattern in the ID register after filtering, AND
- the DLC of received CAN data frame is exactly matching the configured DLC, AND
- If DLC ≠ 0000, the data field of received frame has at least one bit set in a bit position which corresponds to a set bit in the configured data mask, AND
- A CRC field has been received, including a recessive CRC delimiter, and no error is detected prior to the ACK slot.

The CA-IF1145 has a frame error counter. This error counter determines the CAN frame errors detected by the device. The initial counter value is zero, if the device receives a CAN message with errors (like stuffing error, CRC error or CRC delimiter error) prior to ACK slot, the internal error counter is incremented by 1. If a received CAN message without any errors prior to ACK slot, the counter is decremented by 1 in case of the counter is not zero. Any message received after the CRC delimiter or before the next start of frame (SOF) will be ignored by partial networking and has no impact on the frame error counter. The default value for the frame error counter threshold is 31, so the frame overflow flag PNFDE is set once the counter > 31, a frame detect error is captured (PNFDE = 1) and the device wakes up. The counter will be reset to zero when the transceiver switches to offline mode or partial networking is enabled again. Every time when the error counter is decremented or incremented, device will wait for $n_{bit(idle)}$ recessive bits before considering a dominant bit as a SOF, see Figure 9-7.

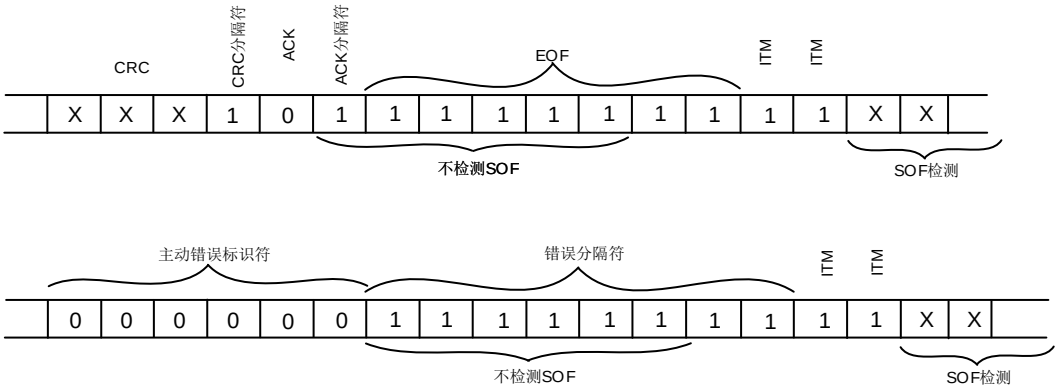


Figure 9-7. SOF detection after Classic CAN frames and error scenarios

If PNCOK is set by the application software, partial networking is assumed to be configured correctly. The CA-IF1145 will clear PNCOK after a write access to any of the CAN partial networking configuration registers, see CAN Partial Networking Configuration Registers section. When the CAN transceiver is in offline mode and CAN remote wake-up is enabled (CWE = 1), but the selective wake-up is disabled (CPNC = 0) or partial networking is not configured correctly (PNCOK = 0), any valid wake-up pattern (WUP) will trigger a wake-up event. If the CAN transceiver is not in offline mode (CMC ≠ 00) or CAN wake-up is disabled (CWE = 0), all wake-up patterns on the bus will be ignored. If both CAN wake-up (CWE = 1) and CAN selective wake-up (CPNC = 1) are enabled, and the partial networking registers are configured correctly (PNCOK = 1), the transceiver will monitor the bus for a dedicated CAN wake-up frames.

The CA-IF1145 supports 50kbps, 100kbps, 125kbps, 250kbps, 500kbps and 1 Mbps bit-rate configured via CDR bits in the data rate control register, 0x26 (Table 9-9) during selective wake-up detection.

9.6. CAN Partial Networking

Partial networking was developed based on the ISO 11898-2:2016 standard. It offers a solution to save power in CAN 2.0 and CAN FD networks by allowing bus communication but sleeping nodes only wake on a specific CAN message or frame. With this additional feature of partial networking, the CA-IF1145 is ideal for the CAN FD and standard CAN 2.0 mixed networks and benefits the network to only enable needed nodes while the rest are in a low power sleep mode without generating bus errors. This is especially important in an automotive setting communications.

As mentioned in Selective Wake-up section, when both CAN wake-up (CWE = 1) and CAN selective wake-up (CPNC = 1) are enabled, and the partial networking registers are configured correctly (PNCOK = 1), the high-speed transceiver will monitor the bus for a dedicated CAN wake-up frame(WUF).

9.6.1. CAN FD Frame Tolerance

The ISO 11898-2:2016 standard includes the physical layer for high-speed CAN, CAN FD and partial networking. To avoid complicated data decoding operation, partial networking uses high-speed CAN for waking up evaluation. After CAN FD was introduced into the automotive market, all CAN controllers are required to comply with the new standard (FD-active) or at least to tolerate CAN FD communication (FD-passive).

The CA-IF1145 can be configured to recognize CAN FD frames as valid frames. When CFDC = 1 (Table 9-6), the CA-IF1145 decrements error counter every time the control field of a CAN FD frame is received; When CFDC = 0, the CA-IF1145 treat CAN FD frames as error frames and increment the error counter, this will accumulate the error counter that can overflow and set PNFDE bit, cause a wake-up. As the CAN-FD frame format is different from high-speed CAN frame format, CAN FD frames will never be recognized as valid wake-up frame even if PNDM = 0 (

Table 9-12) and the frame contains a valid ID. After receiving the control field of a CAN FD frame, the CA-IF1145 ignores the remaining part of CAN-FD frame by waiting for the next bus idle ($n_{bit(idle)}$ recessive bits).

There are two bit-filter options available to support different combinations of arbitration and data bit-rates:

- Dominant bit-filter 1 ($t_{filtr(bit)dom1}$): data bit-rate ≤ 4 x arbitration-rate, support a maximum data bit-rate of 2 Mbit/s and a maximum arbitration speed of 500 kbit/s;
- Dominant bit-filter 2 ($t_{filtr(bit)dom2}$): data bit-rate ≤ 10 x arbitration-rate, or 5 Mbps whichever is lower shall be supported.

The dominant bit filter CAN be configured through the FD_FL bit in the CAN transceiver data rate register (25h). When CFDC=0, the CAN FD frame is understood as an error. Therefore, the error counter increases after receiving the CAN FD. When the ratio of CAN FD frames to valid CAN frames exceeds a certain threshold to the extent that the error counter is overloaded, PNFDE is set to 1 and the device is awakened.

9.6.2. CAN Partial Networking Configuration Registers

Table 9-9. Data rate control register (address = 0x26)

Bit	Symbol	Type	Value	Description
7:3	Reserved	R	-	
2:0	CDR	R/W		CAN data-rate selection
			000	50 kbps
			001	100 kbps
			010	125 kbps
			011	250 kbps
			100	Reserved
			101	500 kbps
			110	Reserved
			111	1000 kbps

Table 9-10. Partial networking ID register (address = 0x27– 0x2A)

Address	Bit	Symbol	Type[1]	Value	Description
27h	7:0	ID7:ID0	R/W		extended frame format: ID7 to ID0
28h	7:0	ID15:ID08	R/W		extended frame format: ID15 to ID8
29h	7:2	ID23:ID18	R/W		extended frame format: ID23 to ID18 standard frame format: ID5 to ID0
	1:0	ID17:ID16	R/W		extended frame format: ID17 to ID16
2Ah	7:5	Reserved	R	-	
	4:0	ID28:ID24	R/W		extended frame format: ID28 to ID24 standard frame format: ID10 to ID6
Note: R = Read only; R/W = Read and Write; X= Don't care.					

Table 9-11. Partial networking ID mask register (address = 0x2Bh – 0x2E):

Address	Bit	Symbol	Type	Value	Description
2Bh	7:0	M7:M0	R/W		extended frame format: mask for ID bits 7 to 0
2Ch	7:0	M15:M8	R/W		extended frame format: mask for ID bits 15 to 8
2Dh	7:2	M23:M18	R/W		extended frame format: mask for ID bits 23 to 18 standard frame format: mask for ID bits 5 to 0
	1:0	M17:M16	R/W		extended frame format: mask for ID bits 17 to 16
2Eh	7:5	Reserved	R	-	
	4:0	M28:M24	R/W		extended frame format: mask for ID bits 28 to 24 standard frame format: mask for ID bits 10 to 6
Note: R=Read only; R/W= Read and Write; X= Don't care.					

Table 9-12. Frame control register (address = 0x2F)

Bit	Symbol	Type[1]	Value	Description
7	IDE	R/W		partial networking identifier format
			0	standard frame format (11-bit)
			1	extended frame format (29-bit)
6	PNDM	R/W		mask for partial networking data
			0	ignore data length code and data field at wake-up
			1	detect data length code and data field at wake-up
5:4	Reserved	R	-	
3:0	DLC	R/W		number of data bytes expected in a CAN frame
			0000	0 bytes

			0001	1 bytes
			0010	2 bytes
			0011	3 bytes
			0100	4 bytes
			0101	5 bytes
			0110	6 bytes
			0111	7 bytes
			1000	8 bytes
			1001 to 1111	8 bytes

Note:
1. R: Read only; R/W: Read and Write; X: Don't care.

Table 9-13. Data mask registers [2] (address = 0x68 – 0x6F)

Address	Bit	Symbol	Type[1]	Value	Description
68h	7:0	DM0	R/W		Data mask 0 configuration
69h	7:0	DM1	R/W		Data mask 1 configuration
6Ah	7:0	DM2	R/W		Data mask 2 configuration
6Bh	7:0	DM3	R/W		Data mask 3 configuration
6Ch	7:0	DM4	R/W		Data mask 4 configuration
6Dh	7:0	DM5	R/W		Data mask 5 configuration
6Eh	7:0	DM6	R/W		Data mask 6 configuration
6Fh	7:0	DM7	R/W		Data mask 7 configuration

Note:
1. R: Read only; R/W: Read and Write; X: Don't care.
2. All data mask bits are set to 1 by power-on reset default.

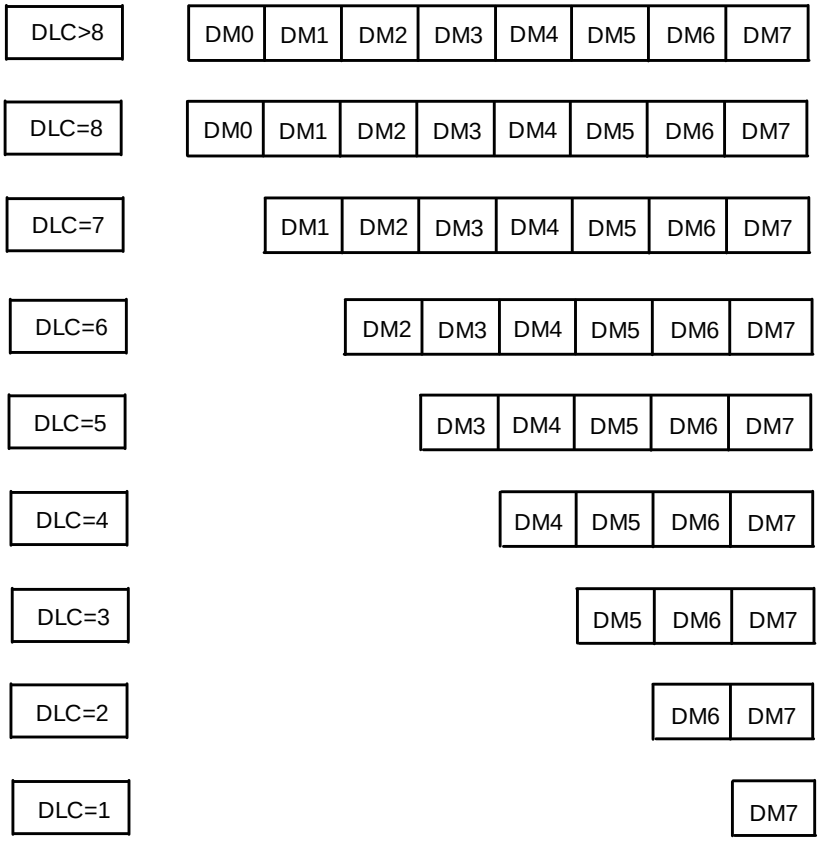


Figure 9-8. Data mask register configuration

9.7. Interrupt and Wake-up Event Diagnosis

9.7.1. Interrupt Sources Detection

RXD and INH pins can be used as an interrupt for the external microcontroller when a wake-up event occurred or an interrupt source triggered. The CA-IF1145 provides wake-up and interrupt event diagnosis. This kind information is stored in the event status registers, see Table 9-16 to Table 9-19. The power-on (PO) and partial networking frame detection error (PNFDE) interrupt sources are always be enabled, other interrupt sources are maskable, wake-up detection can be enabled/disabled in the event capture enable registers. The relevant event status bit is set when an event occurs (if enabled). The microcontroller can monitor events/interrupt sources by reading the event status registers through SPI interface. A global event status register (Table 9-16 错误!未找到引用源。) is provided to speed-up software polling routines and determine the type of event captured (internal controller, transceiver or wake-up interrupts), then access the relevant register as needed. Once an interrupt source has been identified, the status flag should be cleared by writing 1 to the relevant register bit, writing 0 will have no effect. A number of status bits can be cleared with a single write operation(writing 1) to all relevant bits. However, we recommend to clear the status bits that were set only when the status registers were last read. This ensures that events triggered just before the write operation are not lost.

If the CA-IF1145 is in standby mode or CAN transceiver is in offline mode, pin RXD is forced LOW to indicate that a wake-up or interrupt event has been detected; If the CA-IF1145 is in sleep mode when an event (except SPIF interrupt) occurs, pin INH is forced HIGH and the device switches to standby mode. When the device is in standby mode or sleep mode, any enabled wake-up event detected will trigger a wake-up. If CAN transceiver is in active or silent mode, both the standard remote wake-up and WUF can not trigger CW interrupt and CW will not be set, a local wake-up on pin WAKE will trigger a wake-up and set CW to 1.

Table 9-14. Regular wake-up events

Symbol	Event	POR(default status)	Description
CW	Standard CAN bus wake-up	disabled	The CA-IF1145 detected a CAN bus wake-up event while the transceiver in offline mode.
WPR	Local wake-up: rising edge	disabled	The CA-IF1145 detected a low to high rising edge on WAKE terminal.
WPF	Local wake-up: falling edge	disabled	The CA-IF1145 detected a high to low falling edge on WAKE terminal.

After power-on reset, PO is set to 1 and place pin RXD to low. RXD terminal is released only after PO bit cleared. Therefore, only when the PO is cleared, the CA-IF1145 device can enter sleep mode. Otherwise, sending MC = 001 command through SPI will only place the device into standby mode, not sleep mode. CAN bus silent (CBS bit) is detected only when CBSE = 1 while bus active; If there is no activity on CAN bus for $t_{to(silence)}$, CBS bit is set. CBS doesn't trigger interrupt when the transceiver first enters silent mode after power-on reset. After CAN bus is active, CAN bus silent will trigger interrupt when CBS bit is set. CAN bus failure flag CF is used for the transmitter dominant timeout indication and VCC UVLO event (CMC = 01) indication. Once a transmitter dominant timeout or VCC UVLO condition is detected, CAN bus failure flag (CF) is set to 1. The CA-IF1145 enters sleep mode only after this bit is cleared to zero. In sleep mode, the device can detect SPI failure, but don't trigger wake-up. When the device junction temperature > $T_{th(warn)otp}$ (in normal mode only), if enabled by OTWE, OTE will be set to 1. After clearing this bit to zero, if the junction temperature is still above $T_{th(warn)otp}$, OTW will be set again. See Table 9-15 for more details about the interrupt sources.

Table 9-15. Interrupt sources

Symbol	Event	POR (default status)	Description
PO	Power-on	always enabled	Transceiver exited offline mode after battery supply applied.
OTW	Overtemperature alarm	disabled	Junction temperature > $T_{th(warn)otp}$ (detected in normal mode only)
SPIF	SPI fault	disabled	SPI clock count error, illegal MC code or attempt to write the locked register.
PNFDE	PN frame detection error	always enabled	partial networking frame detection error
CBS	CAN bus silent	disabled	CAN bus remains inactive at least $t_{to(silence)}$ (detected in normal mode and CBSE = 1 only).
CF	CAN bus fault	disabled	One of the following CAN failure detected (not in sleep mode): --Transmitter dominant timeout; -- VCC UVLO event (CMC=01).

9.7.2. Interrupt and Wake-up Delay

When the transceiver is in offline mode, if interrupt resources trigger or wake-up events occur frequently, this may cause significant impact on the software processing, because pin RXD will be driven to low level repeatedly and do not have enough time to get response from external microcontroller each time when an interrupt/wake-up is generated. To solve this potential problem, the CA-IF1145 integrates an interrupt/wake-up delay timer to limit the disturbance to the software. When one of the event capture status bits is cleared, pin RXD is released, the timer is reset and start counting. If further events occur while the timer is counting, the relevant status bits will be set to 1. If one or more events are pending when the timer expires after $t_{d(event)}$, pin RXD goes low again to indicate the microcontroller. In this way, the microcontroller is interrupted only once to process a number of events, thus to avoid software processing conflicts. If all active event capture bits have been cleared when the timer expires after $t_{d(event)}$, pin RXD remains high level. The event capture registers can be read at any time.

9.7.3. Event Status Register

Table 9-16 to Table 9-22 show the CA-IF1145 event status and event capture status. Note that, after an event source has been identified, the status flag should be cleared by writing 1 to the correspond status bit.

Table 9-16. Global event status register (address = 0x60)

Bit	Symbol	Type [1]	Value	Description
7:4	Reserved	R	-	
3	WPE	R		WAKE local wake-up event
			0	no local wake-up on WAKE
			1	WAKE local wake-up event pending at address 0x64
2	TRXE	R	-	transceiver event
			0	no transceiver event
			1	transceiver event pending at address 0x63
1	Reserved	R	-	
0	SYSE	R		system event
			0	no system event
			1	system event pending at address 0x61

Table 9-17. System event status register (address = 0x61)

Bit	Symbol	Type[2]	Value	Description
7:5	Reserved	R	-	
4	PO [1]	R/W		power-on indication
			0	power off
			1	device left off mode after battery power-on
3	Reserved	R	-	
2	OTW	R/W		Overtemperature alarm
			0	junction temperature < $T_{th(warn)otp}$
			1	junction temperature ≥ $T_{th(warn)otp}$
1	SPIF	R/W		SPI failure indication
			0	no SPI failure
			1	detected SPI failure
0	Reserved	R	-	

Notes:
1. PO is cleared when device is forced to sleep mode due to UVLO event. This information could be lost because of UVLO event. Bit NMS, which is set to 0 when device returns to normal operation mode after power-on, this can compensates for PO losing.
2. R: Read only; R/W: Read and Write; X: Don't care.

Table 9-18. Transceiver event status register (address = 0x63)

Bit	Symbol	Type[2]	Value	Description
7:6	Reserved	R	-	
5	PNFDE	R/W		partial networking frame detection error
			0	no error detected
			1	detected partial networking frame error
4	CBS	R/W		CAN bus status
			0	CAN bus active
			1	CAN bus inactive for > $t_{to(silence)}$
3:2	Reserved	R	-	
1	CF [1]	R/W		CAN bus fault
			0	no bus fault
			1	detected bus fault
0	CW	R/W		CAN bus wake-up

			0	no wake-up event
			1	detected CAN wake-up event

Notes:
1. CF is only enabled when CAN transceiver is in active mode. This bit is triggered if transmitter dominant timeout or VCC UVLO event is detected (when CMC = 01).
2. R: Read only; R/W: Read and Write; X: Don't care.

Table 9-19. WAKE wake-up event status register (address = 0x64)

Bit	Symbol	Type [1]	Value	Description
7:2	Reserved	R	-	
1	WPR	R/W		WAKE pin rising edge
			0	No rising edge wake-up on WAKE pin
			1	Detected rising edge wake-up on WAKE pin
0	WPF	R/W	-	WAKE pin falling edge
			0	No falling edge wake-up on WAKE pin
			1	Detected falling edge wake-up on WAKE pin

Note:
1. R: Read only; R/W: Read and Write; X: Don't care.

Table 9-20. System event enable register (address = 0x04)

Bit	Symbol	Type [1]	Value	Description
7:3	Reserved	R	-	
2	OTWE	R/W		overtepmerature alarm enable control
			0	disable overtepmerature alarm
			1	enable overtepmerature alarm
1	SPIFE	R/W	-	SPI failure detection enable control
			0	disable SPI failure detection
			1	enable SPI failure detection
0	Reserved	R	-	

Note:
1. R: Read only; R/W: Read and Write; X: Don't care.

Table 9-21. Transceiver event capture enable control register (address = 0x23)

Bit	Symbol	Type [1]	Value	Description
7:5	Reserved	R	-	
4	CBSE	R/W		CAN bus silent detection enable control
			0	disable CAN bus silent detection
			1	enable CAN bus silent detection
3:2	Reserved	R	-	
1	CFE	R/W		CAN bus failure detection enable control
			0	disable CAN bus failure detection
			1	enable CAN bus failure detection
0	CWE	R/W		CAN bus wake-up detection enable control
			0	disable CAN bus wake-up detection
			1	enable CAN bus wake-up detection

Note:
1. R: Read only; R/W: Read and Write; X: Don't care.

Table 9-22. WAKE pin local wake-up enable register (address = 0x4C)

Bit	Symbol	Type [1]	Value	Description
7:2	Reserved	R	-	
1	WPRE	R/W		WAKE rising edge wake-up enable control
			0	Disable rising edge wake-up detection
			1	Enable rising edge wake-up detection
0	WPFE	R/W		WAKE falling edge wake-up enable control
			0	Disable falling edge wake-up
			1	Enable falling edge wake-up

Note:
1. R: Read only; R/W: Read and Write; X: Don't care.

9.8. SPI Interface

The CA-IF1145 has an SPI compatible interface used to read event or interrupt information, read diagnostic data, and configure all of the registers. Each configuration register can be read back to ensure proper configuration. The CA-I1145 communicates with microcontroller through the SPI-compatible 4-wire serial interface:

- Three inputs: clock input (SCK), chip select (SCSN), and data input (SDI)
- One output: data output SDO

The CA-IF1145 is the slave device in an SPI communication with the microcontroller being the master. The SCSN input is used to initiate and terminate a data transfer. SCK is used to synchronize data movement between the master (microcontroller) and the slave device. SCSN must be low to clock data into or out of the device, and SDI must be stable when sampled on the rising edge of SCK. SDO is stable on the rising edge of SCK. The device ignores all activity on SCK and SDI except when SCSN is low, see Figure 8-9. SPI timing diagram and Dynamic Characteristics to find more details about SPI timing characteristics.

The CA-IF1145 supports 16-bit, 24-bit and 32-bit SPI read/write operation. For the 16-bit read/write operation, SPI communication packet is composed of two serial bytes. The first byte specifies the 7 bits address of the CA-IF1145 internal SPI register to be accessed (read or write) and 1 bit read/write control bit(LSB). The second byte in the packet consists of either the data to be written into the addressed CA-IF1145 SPI register (using SDI), or the data read from the addressed CA-IF1145 SPI register (using SDO). If read/write control bit is "0", the device performs write operation and the designated internal SPI register will be updated with the supplied write data (second data byte); if read/write control bit is "1", the device performs read operation and ignores SDI input data. During SPI data read or data write operation, the contents of the addressed register will be returned via pin SDO.

In 24-bit or 32-bit read/write operation, the register address is automatically incremented, as shown in Figure 9-10. During an SPI data read or write operation, the contents of the addressed register will be clocked out from SDO. If the write address provided does not correspond to a physically available internal register, no internal register update will occur in the SPI write operation and the SPI input data is discarded, also do not assert SPI fault event. During SPI write operation, the device counts the number of SCK pulses. If it is not a multiple of 8 (16, 24 or 32), the SPI input data is discarded and SPI failure event is captured, SPI failure flag bit SPIF is set. In SPI read operation, if more than 32 bits data are clocked into the CA-IF1145 via SDI, the data stream on SDI will be returned via SDO from bit 33 onwards.

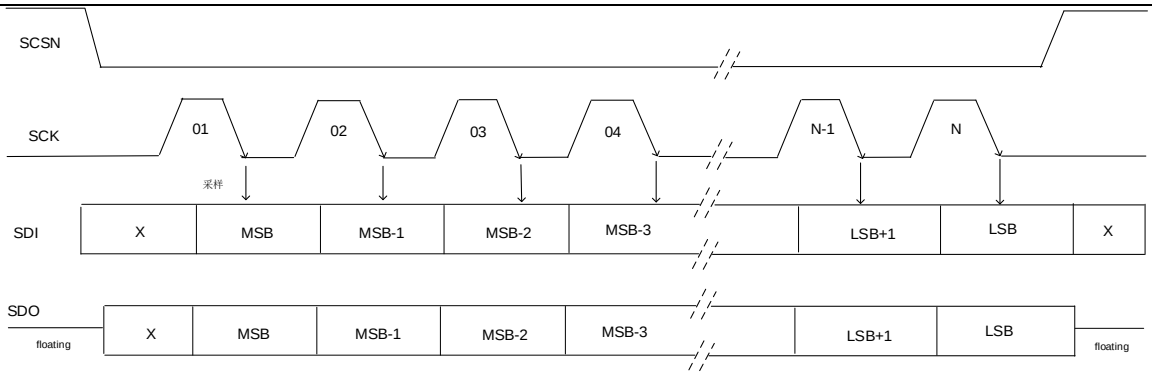


Figure 9-9. SPI communication protocol

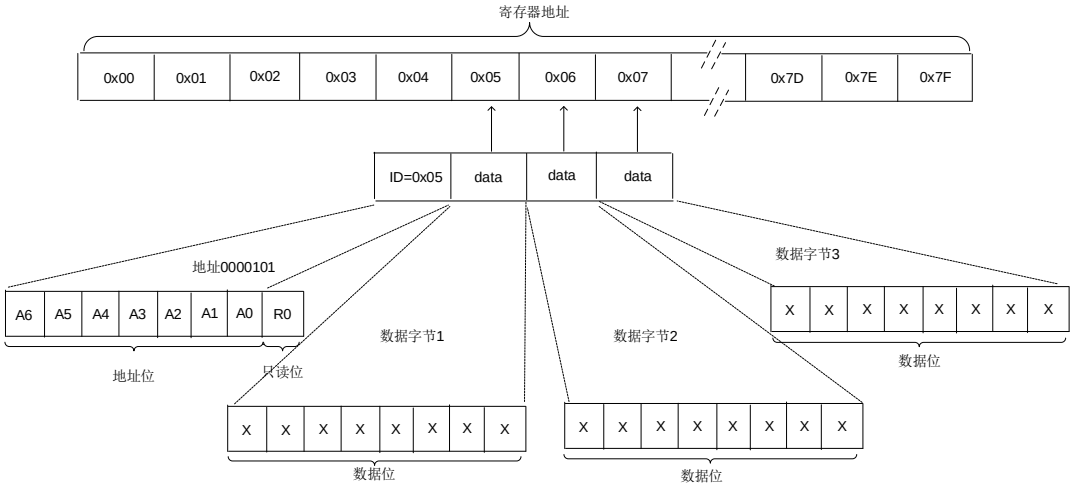


Figure 9-10. SPI write operation

9.9. Register Map and Configuration

9.9.1. Register Map

The CA-IF1145 includes 128 addressable registers with addresses from 0x00 to 0x7F. Table 9-23 shows the register summary and provides descriptions for each bit.

Table 9-23. System control registers summary

Address	Register	Bit							
System control registers									
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x01	Mode control	Reserved					MC		
0x03	Main status	FSMS	OTWS	NMS	Reserved				
0x04	System event enable	Reserved					OTWE	SPIFE	Reserved
0x06	General-purpose register 0[1]	GPM[7:0]							
0x07	General-purpose register 1	GPM[15:8]							
0x08	General-purpose register 2	GPM[23:16]							
0x09	General-purpose register 3	GPM[31:24]							
0x0A	Lock control	Reserved	LK6C	LK5C	LK4C	LK3C	LK2C	LK1C	LK0C
Transceiver control and partial networking registers									
0x20	CAN control	Reserved	CFDC	PNCOK	CPNC	Reserved		CMC	
0x22	CAN transceiver status	CTS	CPNERR	CPNS	COSCS	CBSS	Reserved	VCS	CFS
0x23	Transceiver event enable	Reserved			CBSE	Reserved		CFE	CWE
0x26	Data rate	Reserved					CDR		
0x27	Identifier 0	ID[7:0]							
0x28	Identifier 1	ID[15:8]							
0x29	Identifier 2	ID[23:16]							
0x2A	Identifier 3	Reserved			ID[28:24]				
0x2B	Mask 0	M[7:0]							
0x2C	Mask 1	M[15:8]							
0x2D	Mask 2	M[23:16]							
0x2E	Mask 3	Reserved			M[28:24]				
0x2F	Frame control	IDE	PNDM	Reserved		DLC			
0x68	Data mask 0	DM0[7:0]							
0x69	Data mask 1	DM1[7:0]							
0x6A	Data mask 2	DM2[7:0]							
0x6B	Data mask 3	DM3[7:0]							
0x6C	Data mask 4	DM4[7:0]							
0x6D	Data mask 5	DM5[7:0]							
0x6E	Data mask 6	DM6[7:0]							
0x6F	Data mask 7	DM7[7:0]							
WAKE control and status registers									
0x4B	Pin WAKE status	Reserved						WPVS	Reserved
0x4C	Local wake-up enable	Reserved						WPRE	WPFE
Event Capture registers									
0x60	Event capture status	Reserved				WPE	TRXE	Reserved	SYSE
0x61	System event status				PO	Reserved	OTW	SPIF	Reserved
0x63	Transceiver event status	Reserved		PNFDE	CBS	Reserved		CF	CW
0x64	Pin WAKE status	Reserved						WPR	WPF
Identifier registers									
0x7E	Identifier[2]	IDS[7:0]							

Note:

1. 4 bytes general-purpose memory can be used to store user information.
2. A byte ID is reserved at address 0x7E as CA-IF1145 identification code, the default ID is 74h.

Note that, the CA-IF1145 has 4 bytes of memory for general-purpose registers used to store user information. The general purpose registers can be accessed via the SPI at address 0x06 to 0x09. A byte is reserved at address 0x7E is the CA-IF1145 identification code, the default ID is 74h.

The CA-IF1145 provides a write-protected register to protect against unintended modifications. Note that this facility only protects locked bits from being modified via the SPI and will not prevent the device updating status registers, see Table 9-24.

Table 9-24. Lock control register [1] (address = 0x0A)

Bit	Symbol	Type[2]	Value	Description
7	Reserved	R	-	
6	LK6C	R/W		0x68 to 0x6F partial networking data byte registers lock control
			0	Enable SPI write
			1	Disable SPI write
5	LK5C	R/W		0x50 to 0x5F lock control
			0	Enable SPI write
			1	Disable SPI write
4	LK4C	R/W		0x40 to 0x4F WAKE configuration registers lock control
			0	Enable SPI write
			1	Disable SPI write
3	LK3C	R/W		0x30 to 0x3F registers lock control
			0	Enable SPI write
			1	Disable SPI write
2	LK2C	R/W		0x20 to 0x2F transceiver and partial networking registers lock control
			0	Enable SPI write
			1	Disable SPI write
1	LK1C	R/W		0x10 to 0x1F registers lock control
			0	Enable SPI write
			1	Disable SPI write
0	LK0C	R/W		0x06 to 0x09 registers lock control
			0	Enable SPI write
			1	Disable SPI write

Notes:
1. The CA-IF1145 protects the locked bits from being modified through SPI interface only.
2. R: Read only; R/W: Read and Write; X: Don't care.

9.9.2. Register Configuration

Table 9-25. shows the register configuration status in different mode changes. Some register bits may change state automatically when the CA-IF1145 switches from one operating mode to another, especially when the device switches to off mode because of the battery voltage is too low, or switches to sleep mode because of an UVLO event. If the CA-IF1145 changes operation mode during SPI communication, data transmission will be ignored.

Table 9-25. Register configuration @ different modes

Symbol	Off (POR)[1]	Standby	Normal	Sleep	Overtemperature Protection	Sleep_UVLO[2]
CBS	0	no change	no change	no change	no change	0
CBSE	0	no change	no change	no change	no change	no change
CBSS	1	actual state	actual state	actual state	actual state	actual state
CDR	101	no change	no change	no change	no change	no change
CF	0	no change	no change	no change	no change	0
CFDC	0	no change	no change	no change	no change	no change
CFE	0	no change	no change	no change	no change	no change
CFS	0	actual state	actual state	actual state	actual state	actual state
CMC	01	no change	no change	no change	no change	no change
COSCS	0	actual state	actual state	actual state	actual state	actual state
CPNC	0	no change	no change	no change	no change	0
CPNERR	1	actual state	actual state	actual state	actual state	actual state
CPNS	0	actual state	actual state	actual state	actual state	actual state
CTS	0	0	actual state	0	0	0
CW	0	no change	no change	no change	no change	0
CWE	0	no change	no change	no change	no change	1
DMn	11111111	no change	no change	no change	no change	no change
DLC	0000	no change	no change	no change	no change	no change
FSMS	0	no change	no change	0	no change	1
GPMn	00000000	no change	no change	no change	no change	no change
IDn	00000000	no change	no change	no change	no change	no change
IDE	0	no change	no change	no change	no change	no change
IDS	01110100	no change	no change	no change	no change	no change
LKnC	0	no change	no change	no change	no change	no change
Mn	00000000	no change	no change	no change	no change	no change
MC	100	100	111	001	don't care	001
NMS	1	no change	0	no change	no change	no change
OTW	0	no change	no change	no change	no change	0
OTWE	0	no change	no change	no change	no change	no change
OTWS	0	actual state	actual state	actual state	actual state	actual state
PNCOK	0	no change	no change	no change	no change	0
PNDM	1	no change	no change	no change	no change	no change
PNFDE	0	no change	no change	no change	no change	0
PO	1	no change	no change	no change	no change	0
SPIF	0	no change	no change	no change	no change	0
SPIFE	0	no change	no change	no change	no change	no change
SYSE	1	no change	no change	no change	no change	0
TRXE	0	no change	no change	no change	no change	0
VCS	0	actual state	actual state	actual state	actual state	actual state
WPE	0	no change	no change	no change	no change	0
WPF	0	no change	no change	no change	no change	0
WPFE	0	no change	no change	no change	no change	1
WPR	0	no change	no change	no change	no change	0
WPRE	0	no change	no change	no change	no change	1
WPVS	0	no change	no change	no change	no change	no change

Notes:

1. POR: power on reset or default value;
2. Sleep_UVLO: the device enters sleep mode because of UVLO.

10. Application Information

The CA-IF1145 high-speed CAN transceiver is typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. Figure 10-1 shows the typical application circuit for the CA-IF1145. In Figure 10-1, VIO is connected with +3.3V MCU logic-supply and provides a logic-high output at RXD, SDO and SPI interface with the microcontroller's supply rail. The logic compatibility of RXD, TXD and SPI interface eliminate external logic level translator and longer propagation delay due to level shifting. Connect VIO to VCC to operate with +5V logic systems.

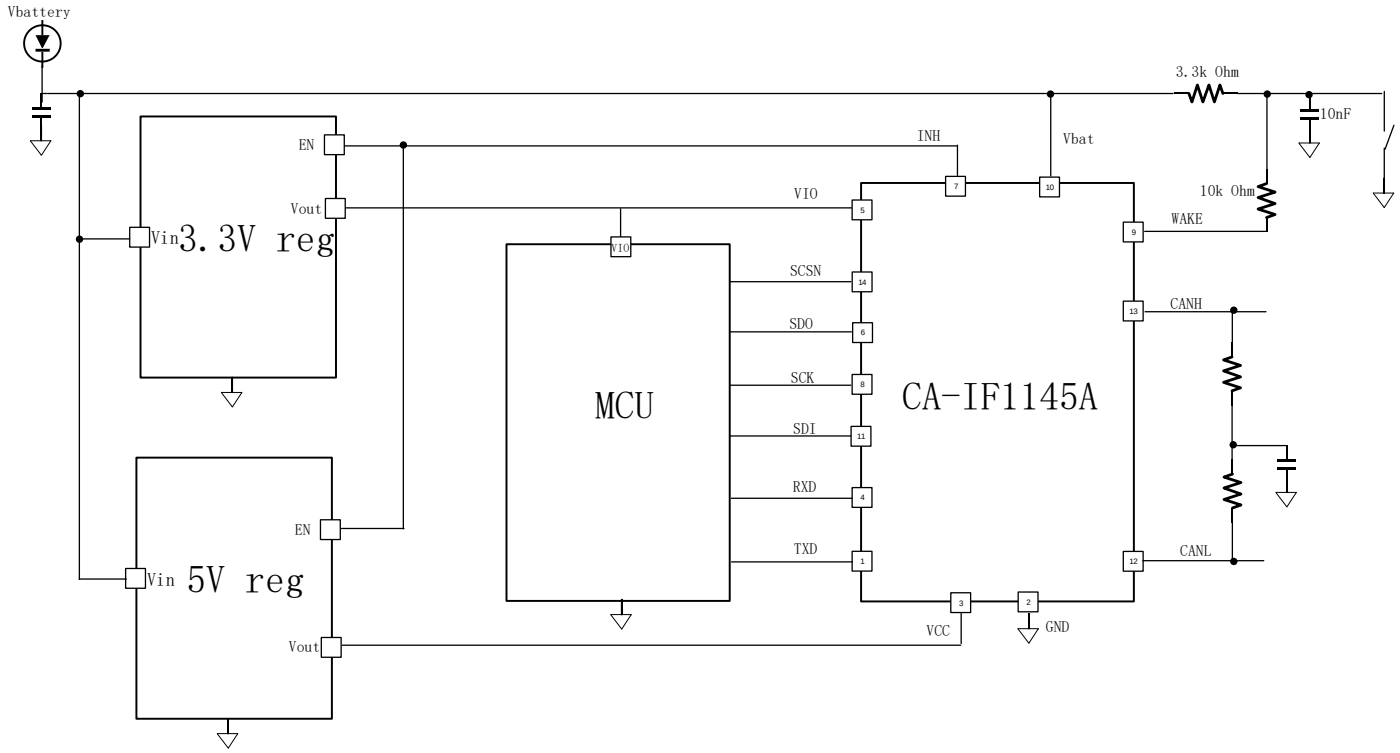


Figure 10-1. CA-IF1145 Typical Application Circuit

11. Package Information

SOIC14 Package Outline

The following figure illustrates the size drawing and recommended pad size of SOIC14 package. All dimensions are in millimeters.

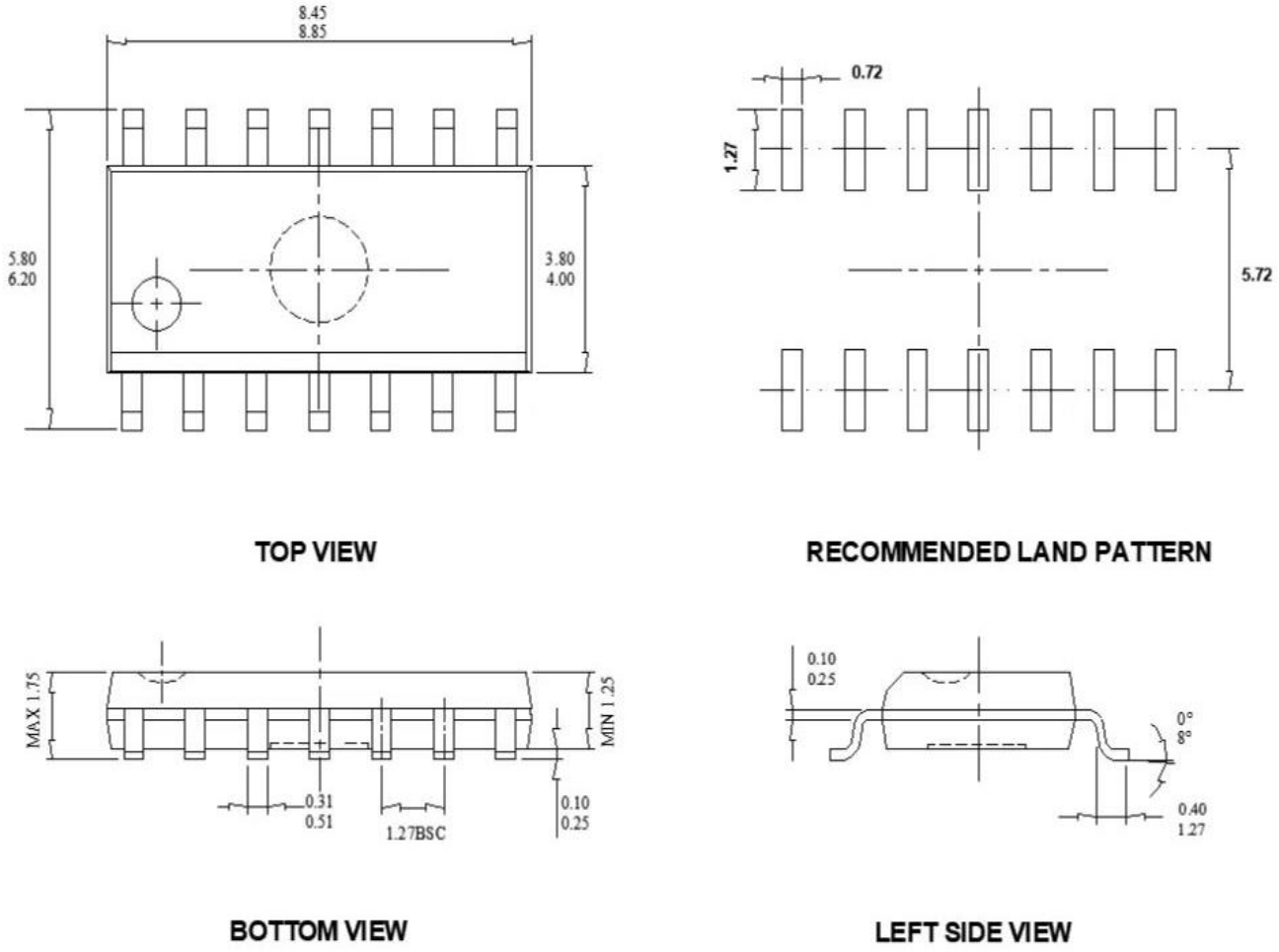


Figure 11-1. SOIC14 package outline

DFN14 Package Outline

The following figure illustrates the size drawing and recommended pad size of DFN14 package. All dimensions are in millimeters.

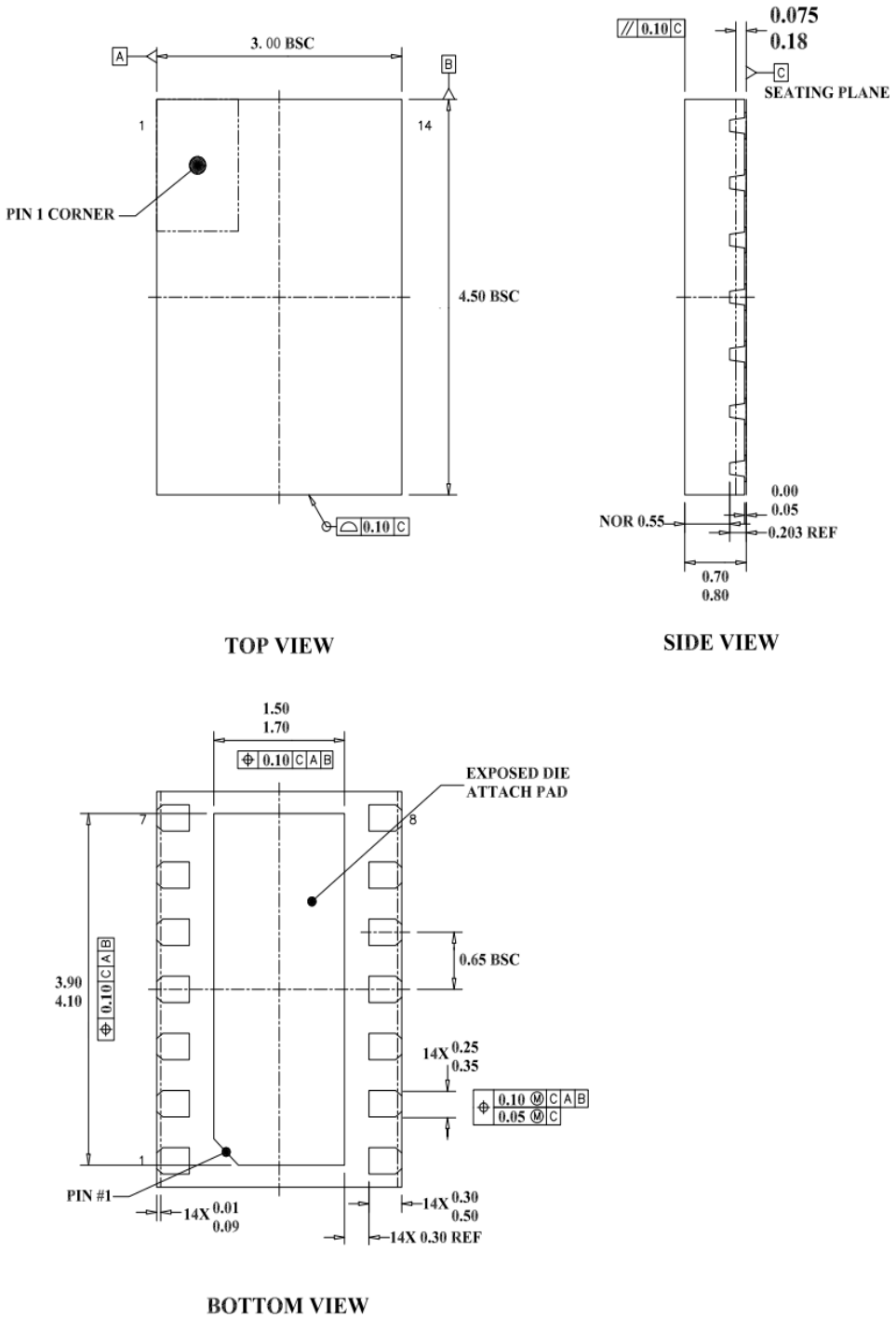


Figure 11-2. DFN14 package outline

12. Soldering Temperature (reflow) Profile

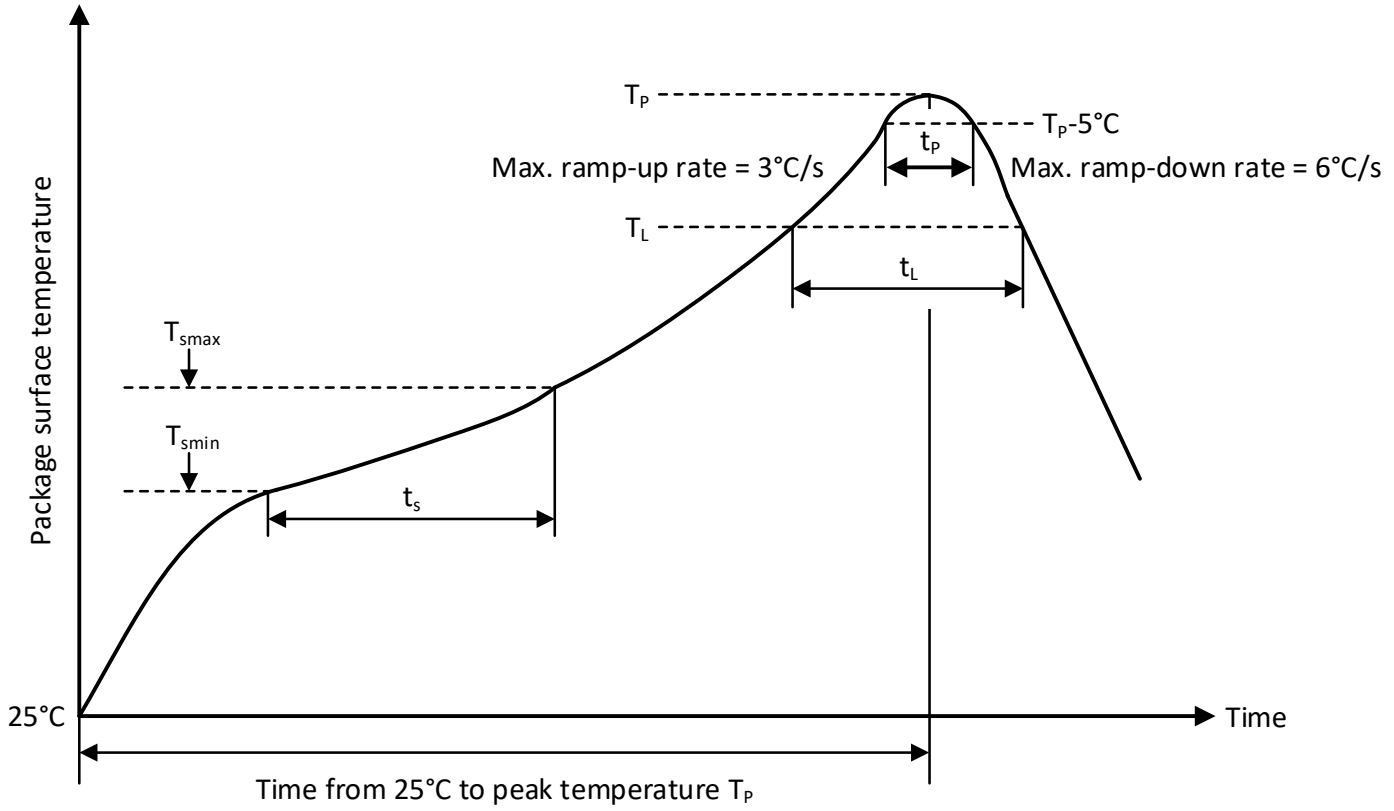


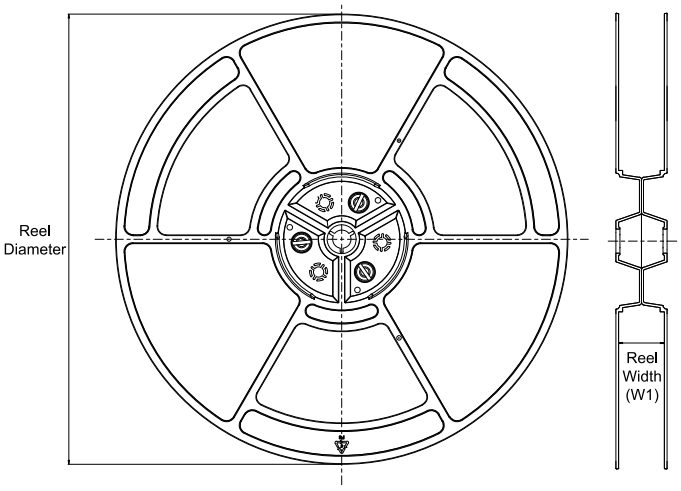
Figure 12-1. Soldering Temperature (reflow) Profile

Table 12-1. Soldering Temperature Parameter

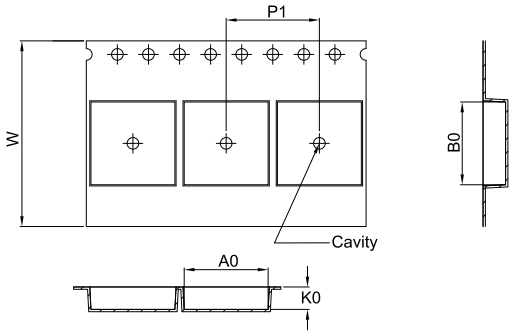
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217°C to Peak)	3°C /second max
Time of Preheat temp(from 150°C to 200°C	60-120 second
Time to be maintained above 217 °C	60-150 second
Peak temperature	260 +5/-0°C
Time within 5°C of actual peak temp	30 second
Ramp-down rate	6 °C /second max.
Time from 25 °C to peak temp	8 minutes max

13. Tape and Reel Information

REEL DIMENSIONS

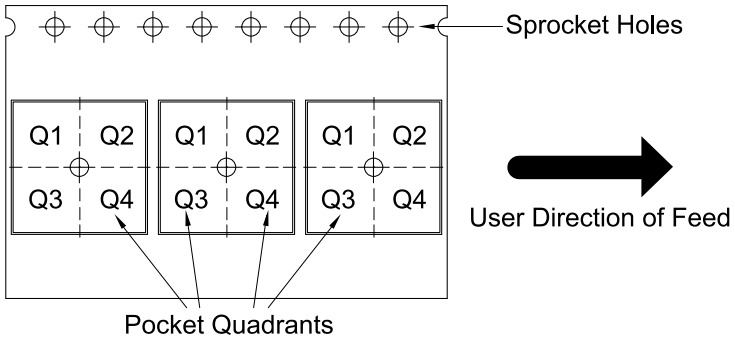


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IF1145NF-Q1	SOIC	NF	14	2500	330	16.4	6.50	9.00	2.10	8.00	16.00	Q1
CA-IF1145FNF-Q1	SOIC	NF	14	2500	330	16.4	6.50	9.00	2.10	8.00	16.00	Q1
CA-IF1145DF-Q1	DFN	DF	14	3000	330	12.4	3.30	4.80	1.10	8.00	12.00	Q1
CA-IF1145FDF-Q1	DFN	DF	14	3000	330	12.4	3.30	4.80	1.10	8.00	12.00	Q1

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